Final Report

(Contract NAS 5-10225)

NONDISSIPATIVE OPTIMUM CHARGE REGULATOR ADVANCED STUDY

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1. INTRODUCTION

This report is a summary of the efforts and achievements during a one year study program in the design, development, and testing of multiphase optimum charge regulators. This program was authorized by the National Aeronautics and Space Administration, under Contract No. NAS 5-10225 and represents a continuation of the work done on Contract No. NAS 5-9210. The previous effort was concerned with the development of the basic circuits required for the efficient transfer of power from a spacecraft solar panel to a spacecraft type battery. This concept of power transfer is described in Section 2. The purpose of this additional work program was improvement of the basic designs with the goal of increasing their efficiency and reliability. Under the continuation program, the level of research and development effort was expanded to include the following:

1. Design, construct, and test a two phase and a four phase optimum charge regulator to demonstrate the feasibility for improved efficiency and reliability.
2. Perform worst case and failure mode analyses on all circuits in order to determine reliability problem areas.
3. Study third electrode charge control devices and their application to optimum charge regulators.
4. Construct mathematical models for each circuit block to indicate critical design areas and demonstrate where redundancy may best be employed.
5. Study all aspects of multiple phase regulators with particular attention to continued operation in the event that one phase becomes inoperative.

1.1 SUMMARY OF EFFORT DURING THE PROGRAM

The initial activity of the program was the redesign of the regulators originally prepared for Contract NAS 5-9210. The 50-watt single phase regulator was modified to include a two-phase switching circuit, and the 250-watt two phase regulator was expanded to a four-phase switching circuit. The remaining circuits in the control loop were simplified to increase their efficiency and reliability, and to reduce the total parts count. The switching transformers were redesigned in an effort to reduce the core losses. These losses were a predominant factor in the inefficiency of the overall system. Photographs of these breadboards are shown in Figures 1-1 and 1-2.

With the exception of the additional phases, the operation of the basic switching circuit and the duty factor modulator circuit is the same as described in the original design. A detailed discussion of these concepts was presented in the original report, and may also be found in Section 2 of this report. This discussion outlines the operational theory of optimum charge regulation, and presents objectives and specifications for the design of this type regulator.

The output characteristics of third electrode cells were examined under various charge and discharge conditions. The results of this study were used to design a control circuit for the 250 watt OCR. Laboratory tests were conducted to verify proper operation.

Mathematical models were constructed for all the circuit blocks. A computer aided worst case analysis was performed, utilizing the models to represent the circuit blocks. Failure mode and stress analyses were also completed on all circuit blocks. Several changes were initiated based on the results of these analyses.

In the case of one phase becoming inoperative, tracking of the maximum power point was accomplished by the remaining phases. However, this condition imposes increased demands upon the remaining phases. To maintain reliable operation in the event of a single phase failure, it is required that the original individual phase design be oversized to handle the increased current and power levels. As the number of phases is increased, this oversize requirement is reduced.

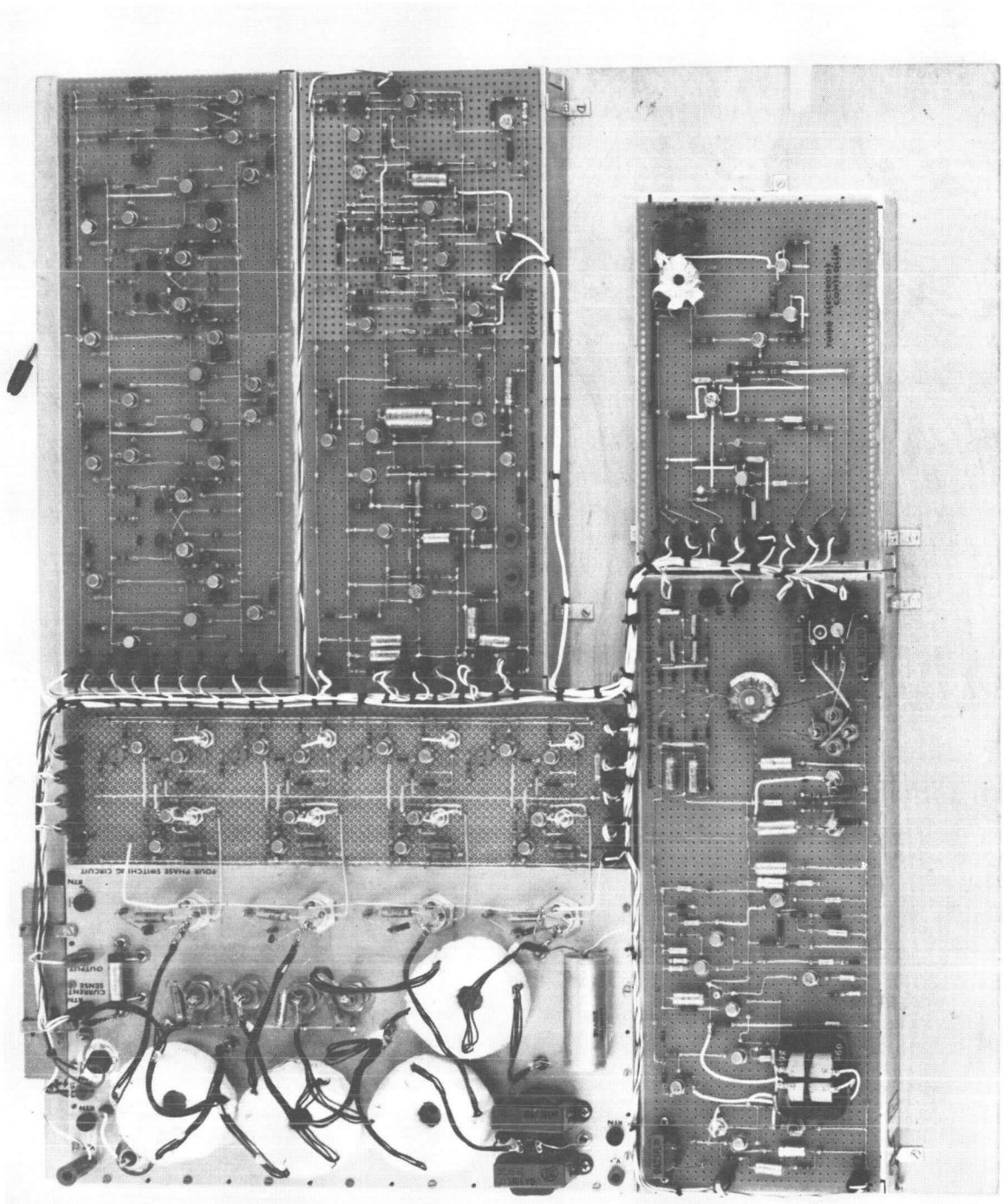


Figure 1-2. 250 Watt Four Phase OCR Breadboard

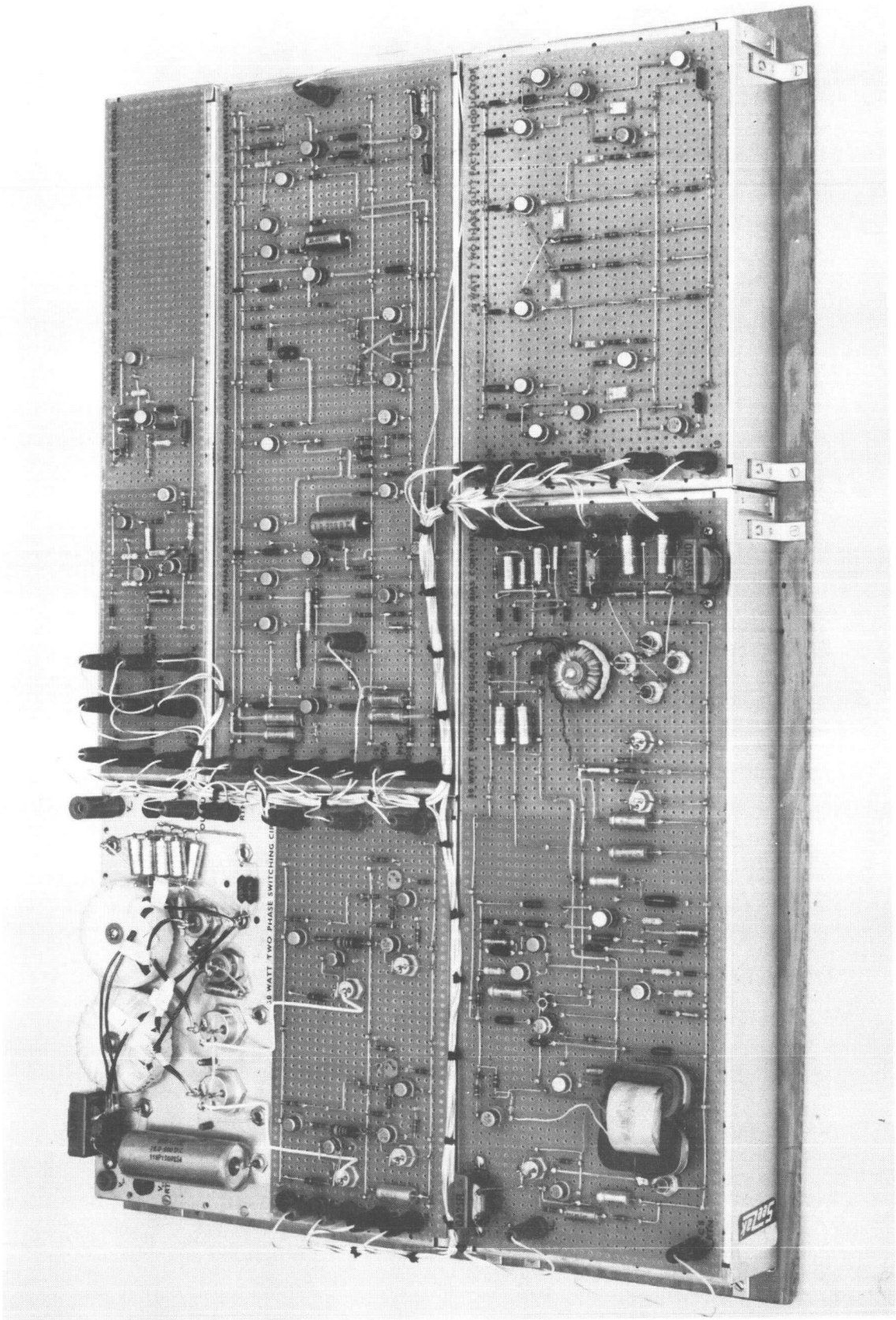


Figure 1-1. 50 Watt Two Phase OCR Breadboard

1.2 SUMMARY OF RESULTS

Testing of the 50 watt and 250 watt regulators at room temperature indicated satisfactory operation over all the extremes of input and output conditions, including the -30 percent power transient. Stable tracking of the maximum power point was observed under the foregoing condition.

Efficiency measurements indicated that the 50 watt regulator exceeded the goal of 85 percent. The 250 watt regulator reached 88 percent, which was very close to the goal of 90 percent. The 250 watt unit was also tested at temperatures of -40°C and +70°C. The efficiency at both temperatures was 88 percent, indicating no loss of efficiency over this temperature range.

A study of third electrode output characteristics was conducted under various charge-discharge conditions. The response time of the output was found to be exceedingly slow; however, a circuit was devised to use this output to effectively control the charge to the battery and to change the mode of operation of the system. Section 3 summarizes this effort.

The worst case, stress, and failure mode analyses resulted in several changes of component values and component ratings. These analyses also indicated critical areas from a reliability standpoint, and appropriate changes are noted for improved reliability. The MTBF for the 50 watt regulator is 22,700 hours based on the Parts Count Prediction and 31,600 hours based on the Failure Mode Analysis. The MTBF for the 250 watt regulator is 15,900 hours based on the Parts Count Prediction, and 27,200 hours based on the Failure Mode Analysis. A detailed summary is presented in Sections 4 and 5.

1.3 TRANSFORMER CONSIDERATIONS

A significant improvement in efficiency resulted from improved switching transformer design. Use of powdered iron cores in the transformer construction allowed the switching circuits to be compensated, such that a resistive switching load line was provided,

instead of the previously inductive load line. This decreased the switching losses by a factor of about six. The increase in the number of phases also aided in the efficiency improvement by reducing the peak currents drawn by the switching circuit.

An attempt was made to further reduce the switching losses by using Litzendraht ("Litz") conductors on the switching transformers. Figures 1-3 through 1-5 show waveform comparisons between the transformers wound with transformer wire and the transformers wound with "Litz" wire for phase 1 of the four phase switching circuit. Figure 2-2 illustrates the basic circuit under discussion. There is no clear improvement apparent in the waveforms, and efficiency measurements indicated that using the transformers wound with "Litz" wire reduced the overall efficiency by about one percent. This is probably due to a loss in the coupling efficiency as a result of the winding difficulties incurred with "Litz" wire.

1.4 CONCLUSIONS AND RECOMMENDATIONS

All of the goals of this phase of the Non-dissipative Optimum Charge Regulator study were achieved with the exception of the efficiency requirement in the 250 watt case. The goals reached were:

- Production of a reliable and efficient multiple-phase OCR design. Demonstration of the reliability characteristics of the OCR designs chosen.
- Verification (by mathematical analysis and extensive laboratory testing) of the performance of the OCR under worst-case operating conditions.
- Verification by analysis of the existance of levels of electrical stress consistent with reliable operation.
- Demonstration of complete conformance to performance goals of 50 watt regulator.
- Demonstration of conformance to performance goals of 250 watt regulator, with the exception of the overall efficiency requirement (Required: 90 percent; measured value: 88 percent).

- Verification of the usage of third electrode sensing for control of battery charging levels.

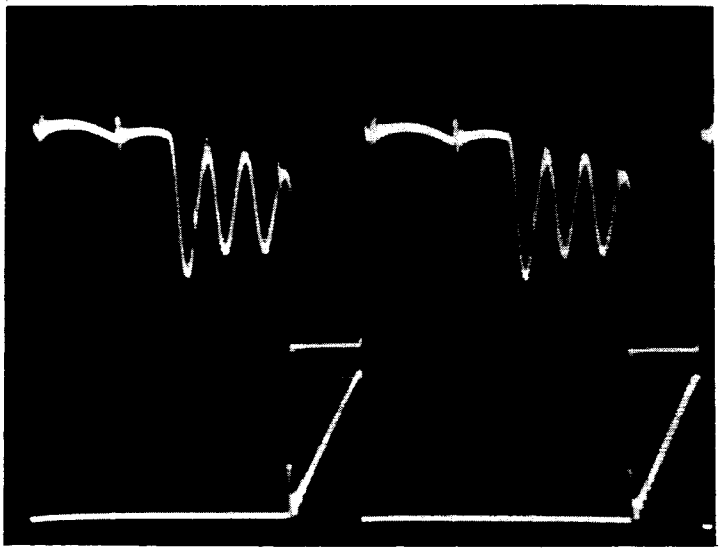
As a direct result of the principles and the feasibility demonstrated in this program, the following recommendations for further application are given:

1. The designs presented are directly applicable to many space mission systems where a highly reliable optimum charge regulator is required. Significant weight and loss savings can be obtained from such usage.
2. The basic power transfer circuitry presented can be used for power conditioning applications requiring high efficiency switching-mode power transfer.

Switching circuit waveforms (transformers wound with transformer wire)

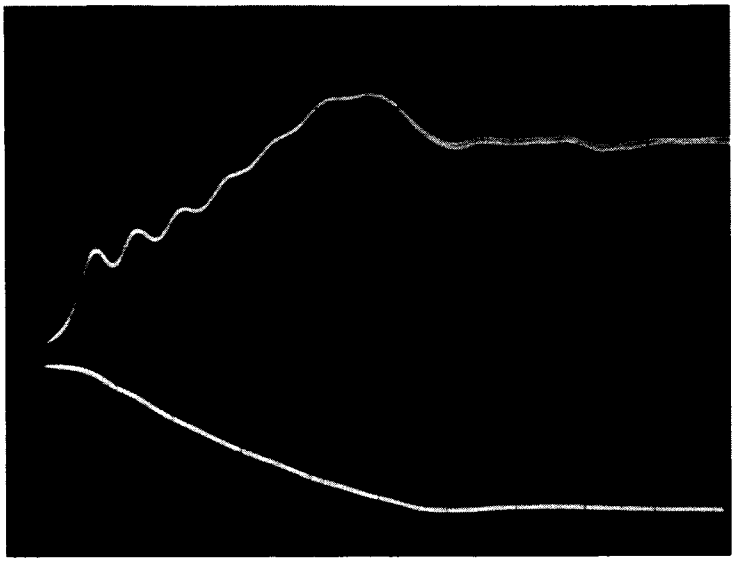
Upper Trace: Vce
Vert: 20v/cm
Horiz: 20 μsec/cm
Lower Trace: Ice
Vert: 5A/cm
Horiz: 20 μsec/cm

Figure 1-3



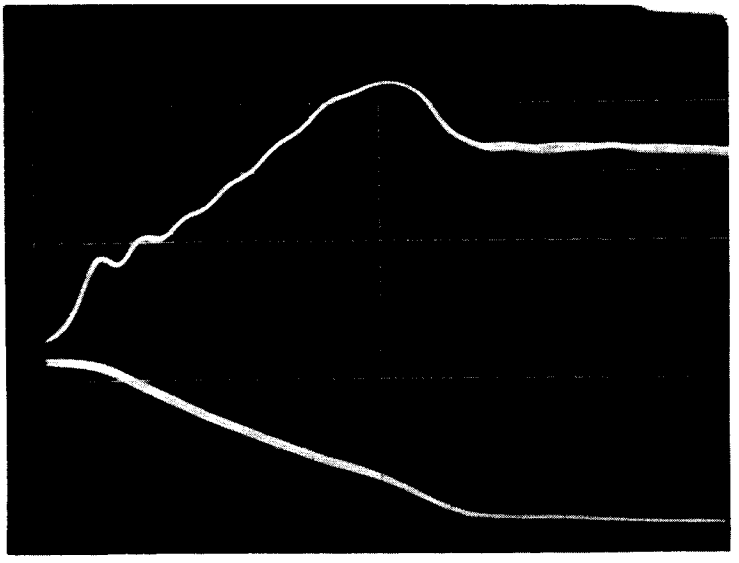
Switching circuit waveforms (transformers wound with transformer wire)

Upper Trace: Vce
Vert: 20v/cm
Horiz: 0.1 μsec/cm
Lower Trace: Ice
Vert: 5A/cm
Horiz: 0.1 μsec/cm
Figure 1-4



Switching circuit waveforms (transformers wound with Litz wire)

Upper Trace: Vce
Vert: 20v/cm
Horiz: 0.1 μsec/cm
Lower Trace: Ice
Vert: 5A/cm
Horiz: 0.1 μsec/cm
Figure 1-5



2. TECHNICAL DISCUSSION

This section is devoted to reviewing the design criteria associated with the concept of power transfer and control. It describes the method of transferring power from the solar panel to the battery, and also describes the technique for optimum control. The design equations for determining all critical circuit parameters are presented.

The basic power transfer and control is performed by a system which can be described by the block diagram of Figure 2-1. The solar panel is coupled to the battery by the power switching circuit. The power transferred by the switching circuit is a function of its switching duty cycle which is controlled by the optimum controller. It senses the battery current and modifies the duty cycle of the switching circuit in a manner which maximizes the battery current.

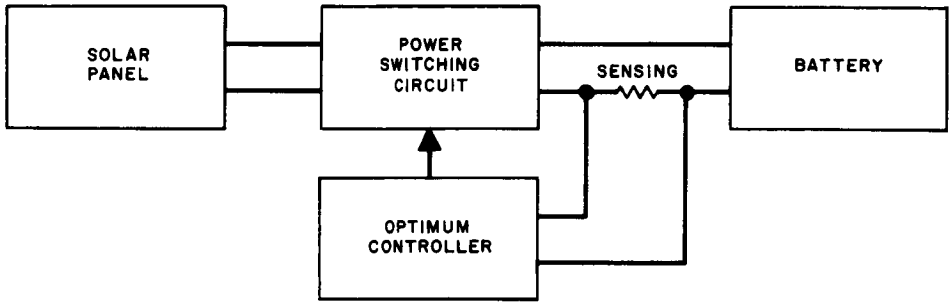


Figure 2-1. Generalized system block diagram.

Two separate cases were considered in the circuit redesign phase of this program. The first was a two phase regulator designed to operate from a 50-watt solar panel. The second was a four phase regulator designed to operate from a 250-watt panel.

The basic concept for both designs was similar except for the fact that the four phase scheme was used in the higher power regulator. This was done to improve the efficiency of this unit and also to improve the ripple filtering characteristics.

Table 2-1 summarizes the specifications for the design of both regulators.

	Case I: 50 Watts	Case II: 250 Watts
Solar Panel Voltage	20 - 30 volts	40 - 50 volts
Solar Panel Current	2.5 - 1.67 amps	6.25 - 5.0 amps
Battery Voltage	12 - 20 volts	25 - 40 volts
Battery Current	3.33 - 2.0 amps	9.0 - 5.63 amps
Efficiency Goal	85 percent	90 percent
Switching Frequency (f_s)	10 kHz	10 kHz
Hunting Frequency (f_H)	150 - 300 Hz	150 - 300 Hz
Hunting Loss Goal	2 percent	2 percent
Power Transient	-30 percent	None
Transient Frequency	10 hz	None
Rise and Fall Time	10 - 20 msec	None
Duty Cycle	50 percent	None

Table 2-1. Summary of Specifications for both cases of the design.

2.1 POWER TRANSFER MECHANISM

The basic mechanism for efficient power transfer from the solar panel to the battery is that of energy storage in an inductor during the first portion of a switching cycle and then the release of this energy to the battery during the next portion of the cycle. The basic switching circuit is shown in Figure 2-2. Q1 is driven by a fixed frequency-variable duty cycle square wave. As the duty cycle is changed, the amount of energy stored in the choke each cycle is changed.

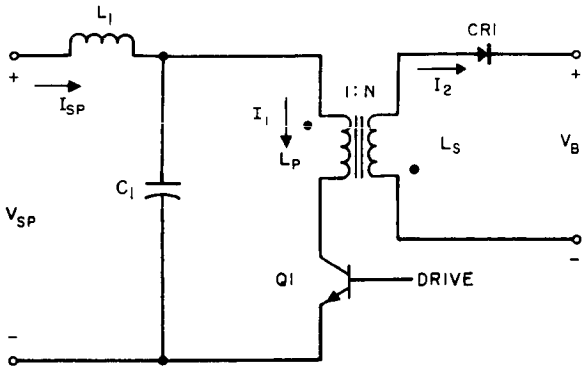


Figure 2-2. Basic switching circuit.

Figure 2-3 shows the current waveforms in both the primary and secondary of the switching choke. As shown by this figure, the current in L_p increases linearly as a function of time and it can be calculated from the relationship.

$$I_1 = \frac{V_{sp}}{L_p} t \qquad (2\text{-}1)$$

For a given duty cycle, D_1, the amount of energy stored in the choke during a single period of oscillation, T, is given by

$$E = 1/2\, L_p \left(\frac{V_{sp}}{L_p} D_1\, T\right)^2 = 1/2\, \frac{V_{sp}^2\, D_1^2\, T^2}{L_p} \qquad (2\text{-}2)$$

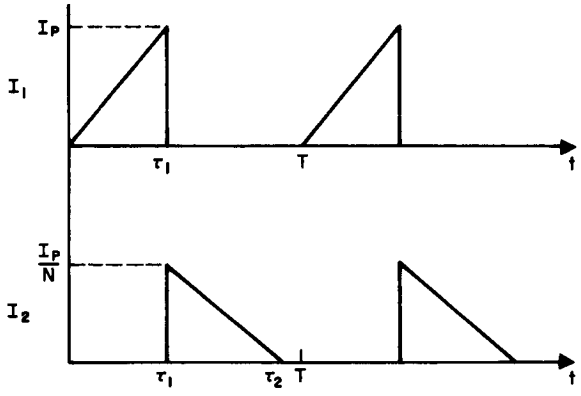


Figure 2-3. Switching circuit current waveforms.

If the energy stored during each cycle is given by the above relationship, then the power absorbed by the choke, and finally delivered to the battery is given by

$$P = E/T = 1/2 \frac{V_{sp}^2 D_1^2 T}{L_p} \quad (2\text{-}3)$$

Since,

$$T = \frac{1}{f_s} \quad (2\text{-}4)$$

where f_s = switching frequency,

then

$$P = 1/2 \frac{V_{sp}^2 D_1^2}{L_p f_s} \quad (2\text{-}5)$$

This relationship defines the amount of power drawn from the solar panel by a single phase regulator such as the 50-watt unit, which was the basis for one of the actual designs. From this equation the solar panel output current can be derived.

Since

$$P = V_{sp} I_{sp} \quad (2\text{-}6)$$

then

$$I_{sp} = 1/2 \frac{V_{sp} D_1^2}{L_p f_s} \quad (2\text{-}7)$$

As shown in Figure 2-3, the secondary current, I_2, is a linearly decreasing ramp beginning at the moment Q_1 turns off. The peak current of this ramp is determined by the peak current of I_1 and the turns ratio of the switching choke. The slope is a function of the battery voltage and the secondary inductance L_s.

$$I_2 = \frac{V_B}{L_s} (t - \tau_1) \quad (2\text{-}8)$$

If circuit losses are neglected, then the power delivered to the battery will be equal to the power drawn from the solar panel.

Therefore,

$$P = \frac{L_s I_2^2}{2T} \tag{2-9}$$

For a given duty cycle $D_2 = (\tau_2 - \tau_1)/T$. The amount of power delivered to the battery is given by

$$P = \frac{V_B^2 D_2^2}{2 L_s f_s} \tag{2-10}$$

From this relationship the average current flowing into the battery is found to be

$$I_2 (AVG) = \frac{V_B D_2^2}{2 L_s f_s} \tag{2-11}$$

The relationship derived in this section define the input and output functions for a single phase switching circuit. These relationships are summarized in Table 2-2. For a multiple phase circuit, the relationships of Table 2-2 can be utilized on a per phase basis. Table 2-3 summarizes the input/output relationships for a multiple phase regulator. The number of phases is given by the symbol ϕ. If $\phi = 1$, the equations of Table 2-2 can be seen to result.

Primary	Secondary
$P = \frac{V_{sp}^2 D_1^2}{2 L_p f_s}$	$P = \frac{V_B^2 D_2^2}{2 L_s f_s}$
$I_{sp} = \frac{V_{sp} D_1^2}{2 L_p f_s}$	$I_2(AVG) = \frac{V_B D_2^2}{2 L_s f_s}$
$I_1(peak) = \frac{V_{sp} D_1}{L_p f_s}$	$I_2(peak) = \frac{I_1(peak)}{N}$

Table 2-2. Single phase switching circuit input/output relationships.

Primary	Secondary
$P = \frac{V_{sp}^2 D_1^2}{2 L_p f_s} \phi$	$P = \frac{V_B^2 D_2^2}{2 L_s f_s} \phi$
$I_{sp} = \frac{V_{sp} D_1^2}{2 L_p f_s} \phi$	$I_2(AVG) = \frac{V_B D_2^2}{2 L_s f_s} \phi$
$I_1(peak) = \frac{V_{sp} D_1}{L_p f_s}$	$I_2(peak) = \frac{I_1(peak)}{N}$

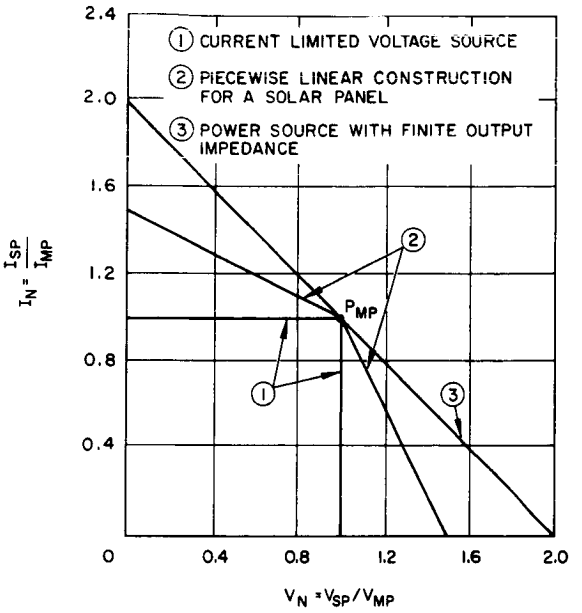
Table 2-3. Multiple phase switching circuit input/output relationships.

The filter L1-C1 is provided to average the switched current I_1. This allows the solar panel to operate at a relatively fixed voltage and current.

2.2 OPTIMUM POWER CONTROL

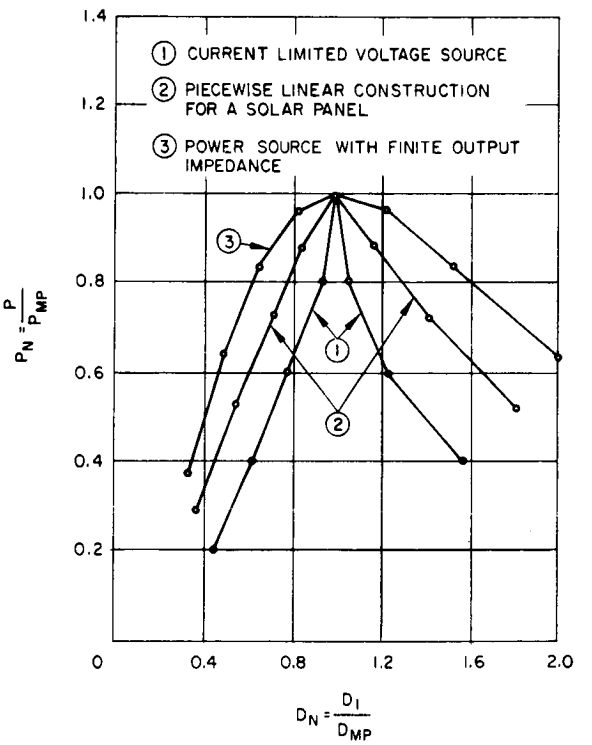
Based on the relationships derived in the last section and summarized in Tables 2-2 and 2-3, it can be seen that the power transferred from the solar panel to the battery will be a function of the duty cycle of Q1. Also of importance is the V-I characteristic of the power source as this will determine the manner by which the power varies as a function of duty cycle.

Figure 2-4 is a plot of the idealized V-I characteristics of various types of power sources. The curves are normalized with respect to the maximum power point. Curve 1 is a representation of a current limited voltage source and curve 3 is that of a voltage source with a finite series impedance. Curve 2 is representative of a multitude of characteristics which could be drawn between the extremes of 1 and 3. Of particular interest is the fact that practical solar panel output characteristics are somewhat between the limits of 1 and 3.



NOTE: V_{MP} AND I_{MP} ARE VOLTAGE AND CURRENT AT THE MAXIMUM POWER POINT

Figure 2-4. Normalized V-I characteristic for various types of power sources.



NOTE: P_{MP} AND D_{MP} ARE VALUES AT THE MAXIMUM POWER POINT

Figure 2-5. Normalized plot of power versus duty factor for the power sources of Figure 2-4.

If all of the parameters are normalized with respect to their values at the maximum point, P_{mp}, as shown in Figure 2-4, then

$$P_n = \frac{P}{P_{mp}} = V_n^2 D_n^2 \qquad (2\text{-}12)$$

where

$$V_n = V_{sp}/V_{mp}$$

$$D_n = D_1/D_{mp}$$

A normalized plot of power versus duty factor is shown in Figure 2-5 for curves 1, 2, and 3. Curve 1 exhibits the most radical change of power for a duty factor variation, while curve 3 shows the most gradual. These curves indicate that in order to maintain very low hunting losses it will be necessary to keep the duty factor variations during the hunting cycle below about 5 percent of D_{mp}. Hunting is the term used for describing the oscillation of the regulator about the maximum power point.

As the duty factor is increased from zero, the maximum power point is eventually reached as shown in Figure 2-5. After this point, the power will begin to decrease again. In terms of the power delivered to the battery,

$$P = V_B I_B \qquad (2\text{-}13)$$

where V_B is the battery voltage and I_B is the average output current of the regulator. Since it is assumed that V_B is a constant for periods of time much greater than the hunting period, the power output is directly proportional to the output current, I_B. Therefore, as the duty factor is changed, the average output current will remain directly proportional to the input power and it will vary in the manner described in the diagram of Figure 2-5. In other words the normalized power may be written as:

$$P_n = KI_B/I_{mp} = KI_n \qquad (2\text{-}14)$$

where K is a constant of proportionality.

Because of this relationship, the output current may be sensed to determine when the regulator is operating at the maximum power point.

2.3 BASIC REGULATOR OPERATION

Based on the results of the preceding section, it can be seen that if the duty factor of the switching circuit is properly adjusted, then the regulator can deliver the maximum available power from the solar panel at all times. It was also shown that the controlling parameter is the average battery current since it is proportional to power. Therefore, a controller which senses the output current and uses this information to control the duty cycle of the switching circuit is the basis for the design.

As shown by the block diagram of Figure 2-6, the control loop which adjusts the duty factor of the switching circuit to the proper value consists of five functional blocks. The output waveforms for each of these blocks are shown in Figure 2-7 and they will be referred to in the following discussion.

If at time t = 0, the regulator is operating at point P_1 of the solar panel characteristic shown in Figure 2-8, and the duty factor is decreasing, the following events will occur. The average value of current flowing into the battery is shown in Figure 2-7a at P_1, and it is increasing towards I_{mp}. At the time that the operating point passes P_{mp} on the solar panel characteristic, the average battery current will reach a maximum and then begin decreasing. The battery current is sensed by a small resistor and then this voltage is amplified by the current sensing amplifier (CSA). The CSA has a low pass characteristic so that it amplifies the average battery current and rejects the switching (carrier) frequency component. The output of the CSA is then fed to the peak holding comparator (PHC) which compares the peak value of the CSA's output to its instantaneous value. When the CSA output has dropped a predetermined ΔV below its peak, a pulse, V_{phc}, is generated as the output of this circuit. This corresponds to the point P_2 in Figure 2-8. The pulse generated by the PHC causes the

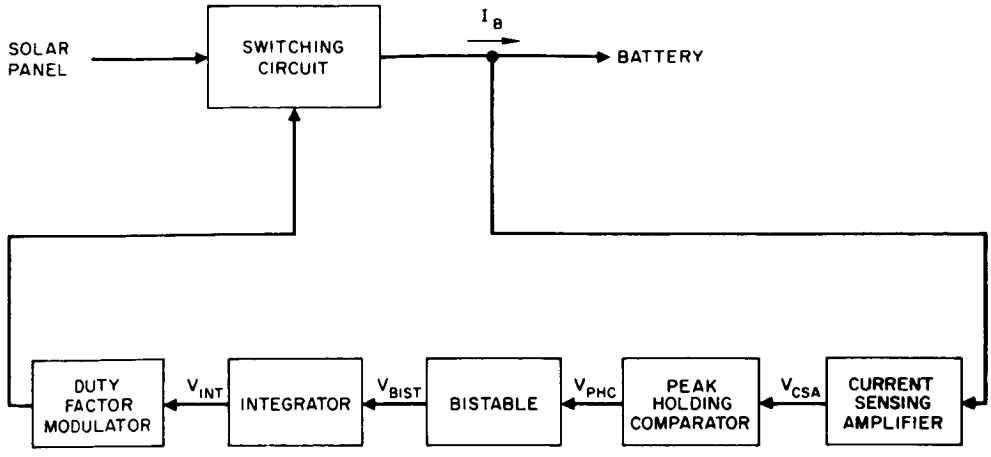


Figure 2-6. Optimum charge regulator block diagram.

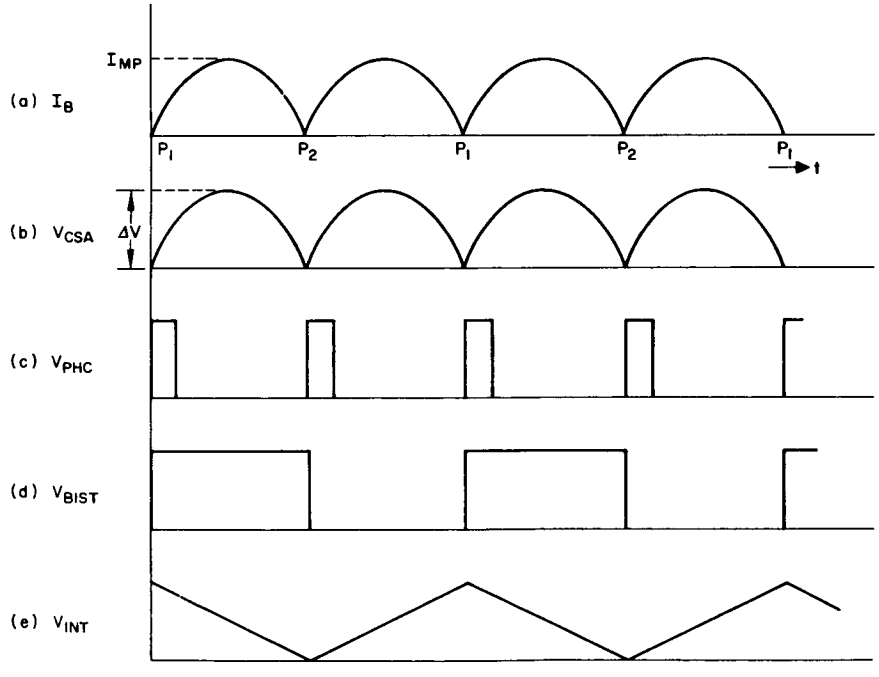


Figure 2-7. Optimum charge regulator control waveforms.

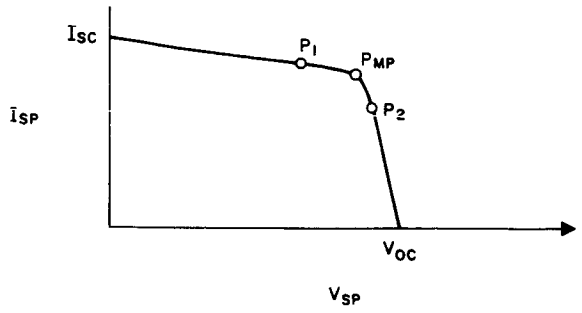


Figure 2-8. Solar panel V-I characteristic.

bistable to reverse states and this causes the integrator to begin increasing the duty cycle. The entire cycle is repeated as the regulator moves its operating point from P2 back to P1. A complete hunting cycle is from P1 to P2 and back to P1.

2.4 HUNTING FREQUENCY

The time required for the regulator to complete one cycle (P1 $\longrightarrow$ P2 $\longrightarrow$ P1) is termed the hunting period or inversely the hunting frequency.

If at time t = 0, the regulator is operating at the maximum power point then the power transferred by a multiple phase regulator can be written as

$$P = \frac{\phi V_{sp}^{\ 2} D_1^{\ 2}}{2 L_p f_s} = \frac{V_B I_B}{\eta} \qquad (2\text{-}15)$$

where

η = regulator efficiency

ϕ = number of phases.

If the duty factor now decreases a small amount then the change in battery current as a function of the change in duty factor and solar panel voltage can be approximated as

$$I_B = \frac{\phi V_{sp} D_1 \eta}{L_p f_s V_B} \left[D_1 \Delta V_{sp} + V_{sp} \Delta D_1 \right] \qquad (2\text{-}16)$$

ΔV_{sp} is a function of the solar panel characteristic and ΔD_1 is a function of the integrator and duty factor modulator circuits. Since the input to the integrator is a step function, its output will have the form

$$\Delta D_1 = kt \tag{2-17}$$

The units of ΔD_1 are volts/second/volt. This is true since the change in duty factor as a function of time is related to the integrator output as a percentage of the peak-to-peak change per switching cycle of the duty factor modulator comparator voltage.

Combining equations 2-16 and 2-17 and solving for the time required for the operating point to shift from P_{mp} to P_2 yields the result

$$t_{p2} = \frac{\Delta I_B L_p f_s V_B - D_1^2 \eta V_{sp} \Delta V_{sp}}{\eta V_{sp}^2 D_1 K\phi} \tag{2-18}$$

It must be noted that since both the duty factor and the average battery current are decreasing, there are negative signs associated with K and ΔI_B.

Assuming complete symmetry for each half cycle ($P_{mp} \longrightarrow P_2 \longrightarrow P_{mp}$ and $P_{mp} \longrightarrow P1 \longrightarrow P_{mp}$) the hunting frequency is found to be

$$f_h = \frac{\eta V_{sp}^2 D_1 K\phi}{4\left[\Delta I_B L_p f_s V_B - D_1^2 \eta V_{sp} \Delta V_{sp}\right]} \tag{2-19}$$

2.5 SWITCHING FREQUENCY SELECTION

There are several criteria for switching frequency selection. Selection of too high a switching frequency will reduce efficiency, while if it is too low, the size and weight will be penalized.

Upon examination of the equations in Tables 2-2 and 2-3, it can be seen that the product of f_s and L_p occurs in all of them. If f_s is decreased with a given solar panel and a fixed maximum power point, then

L_p must be increased or D_1 must be decreased in order to satisfy the equation. An increase in L_p means an increase in size and weight of this component. If D_1 is decreased, the peak current, I_1, increases which results in increased losses.

On the other end of the scale, if f_s is increased, L_p can be decreased thereby reducing its size and weight. However, there are two penalties which result in lowered efficiency. The first is increased core losses in the switching choke due to the increased frequency. The second is due to transistor switching losses. In the worst case the main power transistor, Q_1, has an inductive load line when it turns "off." The waveforms of Figure 2-9 can be used to calculate the switching loss. From these it is found that

$$P_{sw} = I_1(\text{peak}) \left[V_{sp} + \frac{V_B}{N} \right] t_{sw} f_s \qquad (2\text{-}20)$$

where t_{sw} is the voltage rise time and the current fall time for Q_1.

Since t_{sw} is a constant for any given device, P_{sw} will increase as f_s increases. Therefore, proper selection of the switching frequency is necessary to optimize efficiency, size, and weight.

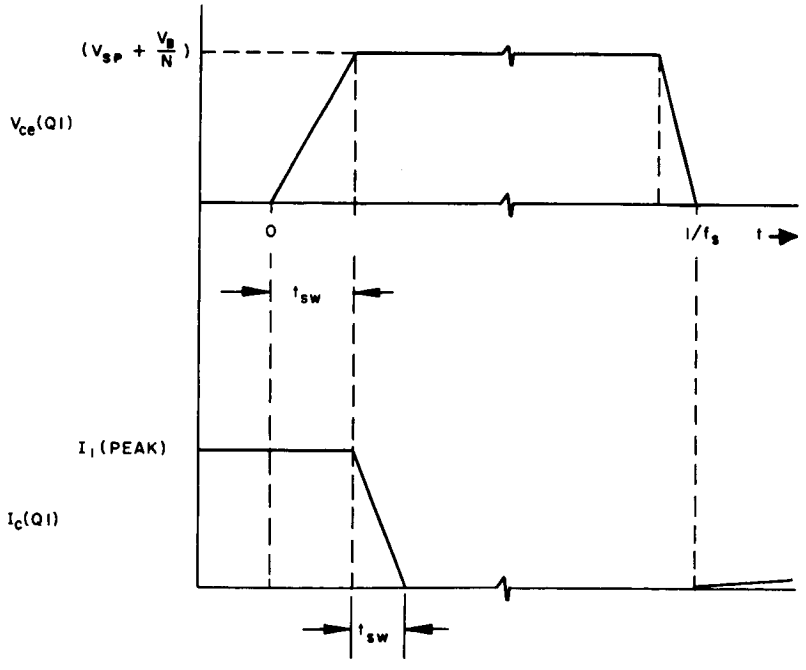


Figure 2-9. Switching transistor waveforms for the switching loss calculation.

3. THIRD ELECTRODE CELL-BATTERY STUDY

The objective of this phase of the OCR study was to investigate the output characteristics of a third electrode (or Adhydrode) in a sealed nickel cadmium cell relative to the state of charge of the cell, and to determine a means to use this output to control the OCR. Many sources have contributed extensive research into the characteristics of nickel cadmium cells, and several sources have done detailed investigations of third electrode characteristics. This study was not intended to further the research of nickel cadmium cells or third electrodes, but to verify the existing results, and to determine a method to utilize these results.

The battery study was divided into four (4) phases, namely:

1. Conditioning and Charging
2. Characteristic Tests
3. Control Circuit Design
4. Testing with the OCR

For these operations a 27 cell battery was constructed. The cells used were produced by Gulton Industries and furnished to this program by N. A. S. A. The battery contained 24 type VO-12HS (12 ampere-hour, hermetically sealed, nickel cadmium) cells, and three (3) type VO-12 HSAD (12 ampere hour, hermetically sealed, nickel cadmium, active Adhydrode) cells. The cells were placed in a battery case and restrained to prevent possible jacket distortion during high current charging (Figure 3-1). The case was constructed with a clear plastic cover (not shown) to provide visual observation during test.

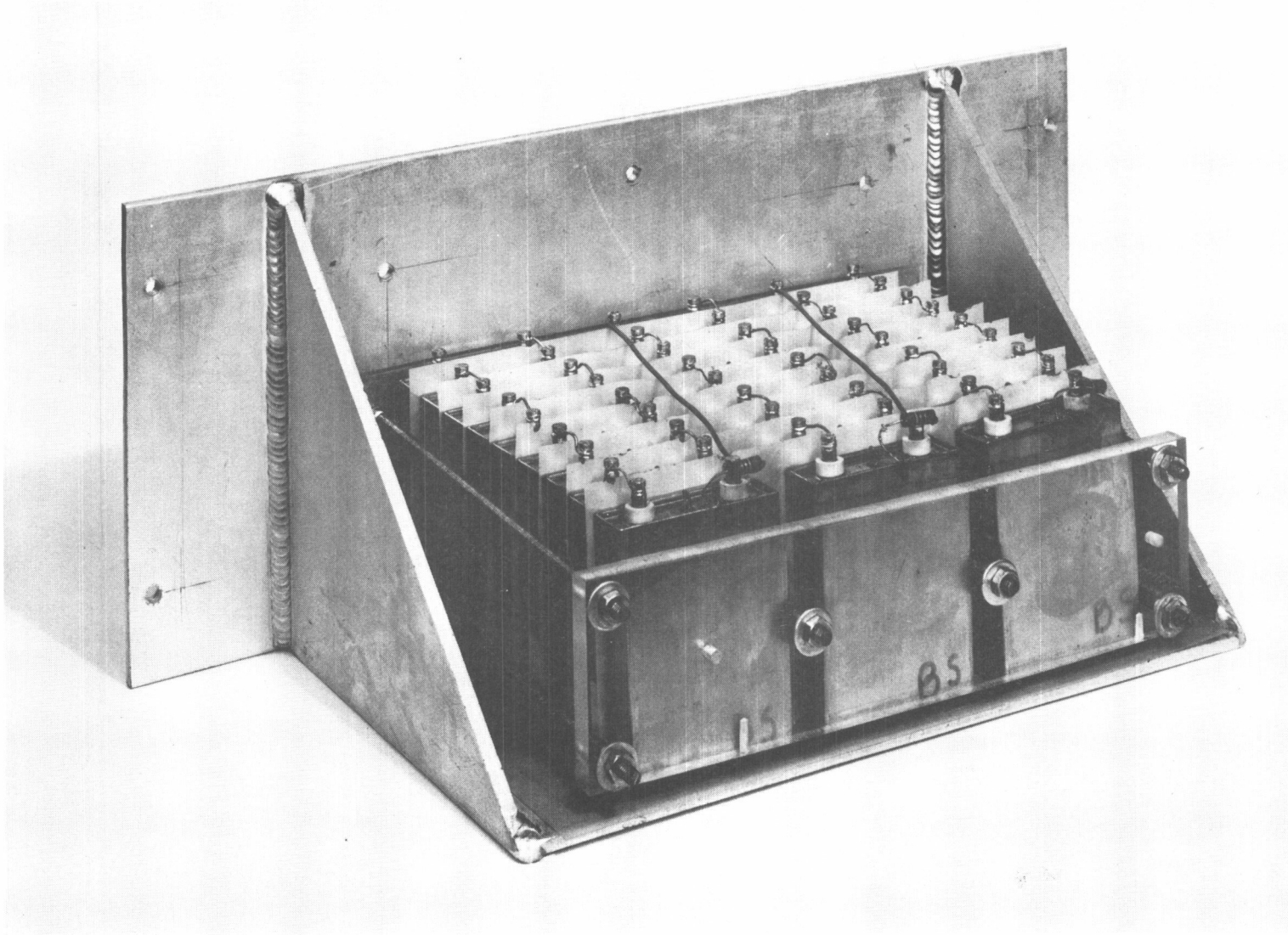


Figure 3-1. 27 cell nickel-cadmium battery with three adhydrode cells.

3.1 THEORETICAL DISCUSSION

The fundamental reactions proceeding within a nickel-cadmium cell may be described by the simplified equation:

$$2Ni(OH)_2 + Cd(OH)_2 \underset{DISCH}{\overset{CHG}{\rightleftharpoons}} 2Ni(OH)_3 + Cd \qquad (1)$$

using an aqueous solution of KOH as an electrolyte.

Within a sealed nickel cadmium cell, there exists an excess of negative material, as compared to positive material. These cells are manufactured such that the positive electrode reaches the charged state first, with relatively little O_2 having been evolved to that point. If the charge current continues after the positive electrode reaches full charge, the positive electrode will give off oxygen while the negative electrode is approaching a charged state. When the charge current is relatively low and the oxygen can return to the negative electrode, the oxygen will recombine with the cadmium and an equilibrium state will occur. If, however, the charge current is high, the rate of disassociation at the positive electrode (oxygen evolved) will be higher than the rate of recombination at the negative electrode (oxygen consumed) and the internal pressure of the cell will increase.

The auxiliary electrode present in the cells used in this program are the Adhydrode, or adsorbed hydrogen type electrode. Essentially this electrode contains hydrogen atoms which react with the oxygen evolved during the charging process, reducing the oxygen by:

$$4H + O_2 \xrightarrow{K} 2H_2O \qquad (2)$$

at a rate proportional to the oxygen pressure within the cell.

$$\frac{dp}{dt} = kP(O_2) \qquad (3)$$

Electrons produced by the charging current travel from the negative electrode thru an external electrical connection (generally resistive) to the Adhydrode where they are consumed by:

$$4H_2O + 4e^- \longrightarrow 4H + 4OH^- \qquad (4)$$

Since hydrogen is removed from the Adhydrode at a rate proportional to the oxygen pressure (3), the electron flow from the negative electrode through the external circuit (to replace the hydrogen) will also have a proportional relationship to the oxygen pressure.

For purposes of illustration, assume that oxygen is evolved from positive electrode at a constant rate (for a given charge current), and that both the negative electrode and the Adhydrode are reducing the oxygen. Then as the negative electrode begins to reach full charge its recombination rate will decrease, and the Adhydrode rate will tend to increase due to the additional oxygen available. This will cause an increase in the electron current through the external circuit (from the negative electrode to the Adhydrode) and this increase could be used to indicate that the battery had reached full charge.

The third electrode provides the additional useful function of reducing the oxygen pressure within the cell (2), thereby reducing the danger of cell rupture during charging operations.

3.2 CONDITIONING AND CHARGING

Before the battery can be used, a conditioning and charging procedure is required to bring the cells up to rated capacity (12 ampere-hours). The procedure necessary for proper conditioning is:

A. Conditioning

1. Discharge
   a. Discharge at C/2 (6.0 amp) rate to an end voltage of 1.0 volts per cell.
   b. Each cell shorted with a 1 ohm resistor for 16 hours.
   c. Each cell dead short for 1 hour.
2. Charge
   a. Charge at C/20 (0.6 amp) rate for 48 hours to a limit of 1.5 volts per cell.
   b. Discharge at C/3 (4.0 amp) rate to an end voltage of 1.0 volts per cell.
   c. Each cell shorted with a 1 ohm resistor for 16 hours.
   d. Each cell dead short for 1 hour.

B. Charging

1. Charge
   a. Charge at C/10 (1.2 amp) rate for 24 hours.
2. Discharge
   a. Discharge at C/2 (6.0 amp) rate to an end voltage of 1.0 volts per cell.
   b. Each cell shorted with a 1 ohm resistor for 16 hours.
   c. Each cell dead short for 1 hour.
3. Repeat B-1
4. Repeat B-2
5. Repeat B-1

The charging current source and discharge current sink is provided by a variable rate – constant current, battery charger/discharger (Figure 3-2). This circuit is designed to sense pre-set voltage limits and automatically changes modes (charge to discharge or vice-versa) when these limits are reached. During the charging cycles, the upper limit was set to trip at 39.15 volts, or at an average of 1.45 volts per cell (to allow for differences between the cells). For discharge cycles, the lower limit was set to 27.0 volts, or 1.0 volts per cell, and cell differences (if any) were ignored.

For the conditioning-charging process, a switch-junction box was constructed to facilitate the changes from discharge to 1 ohm short to dead short and back to charge. Instrumentation was provided to monitor the condition of the cells and the overall battery condition. The third electrodes were returned to the negative electrode through a 6.8 ohm resistor, and their output was also monitored. Figure 3-3 shows the instrumentation points within the battery, and the placement of the third electrode cells. The outputs were recorded on two (2) four (4) channel Sanborn model 150 recorders, using differential input pre-amplifiers. The entire conditioning process required approximately eight (8) days to complete.

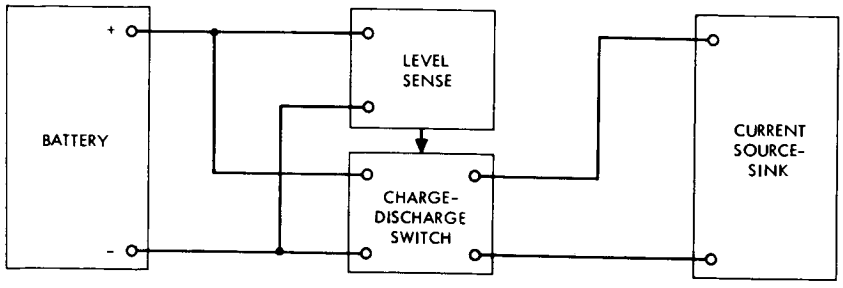
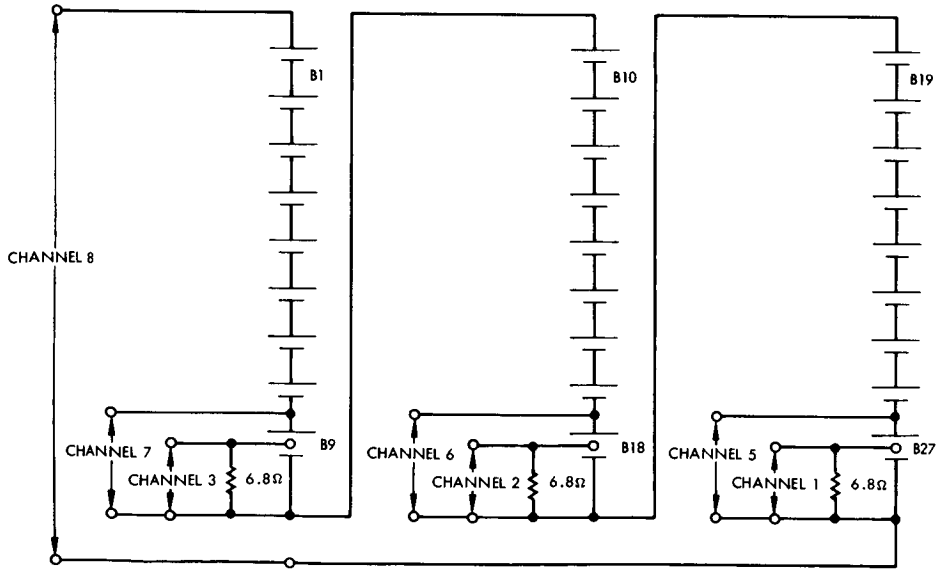


Figure 3-2. Constant current charger – discharger



NOTE: CHANNEL 4 MONITORS CHARGER FOR MODE OF OPERATION

Figure 3-3. Instrumentation points used for conditioning and characteristic tests.

3.3 CHARACTERISTIC TESTS

After the battery was conditioned and charged, a series of tests were performed to determine the output behavior of the third electrode under various charge and discharge rates. Table 3-1 shows the charge-discharge cycles performed. Three complete cycles were performed at each specified charge-discharge rate.

The output of the third electrode was taken across a 6.8 ohm carbon composition resistor connected between the third electrode and the negative electrode of the cell. The 6.8 ohm resistor value was selected based on data obtained from Gulton Industries (the manufacturer) and N.A.S.A. Their curves show that the maximum power can be obtained from the Adhydrode using a resistance value between 6 and 7 ohms, and 6.8 ohms is the only standard carbon composition resistor in this range. Carbon composition resistors were chosen for their inherent reliability and low cost.

The instrumentation employed in these tests is essentially the same as that used in the conditioning-charging phase of the study. In addition, a switch function was employed to allow a Digital Voltmeter (D.V.M.) to be moved from point to point in the battery. Since the accuracy of the recorders is limited, and they seem to experience some reference shift after several hours of operation, the D.V.M. was used to take periodic readings during the cycles. These readings were then compared to the charts produced by the recorders, and the combination reduced to smaller graphs. Figure 3-4 shows the third electrode output and the voltage level of cell Number 9 for tests 1 through 4. Figure 3-5 shows the same curves for tests 5 through 8. The curves show an average set of values from all the cycles that were performed for each combination of charge-discharge rates. The horizontal axis has been normalized by the relation:

$$T = \frac{(\text{Time})\ (\text{Charge Rate})}{(\%\ \text{overcharge})\quad K}$$

where K is arbitrarily chosen to be 3.

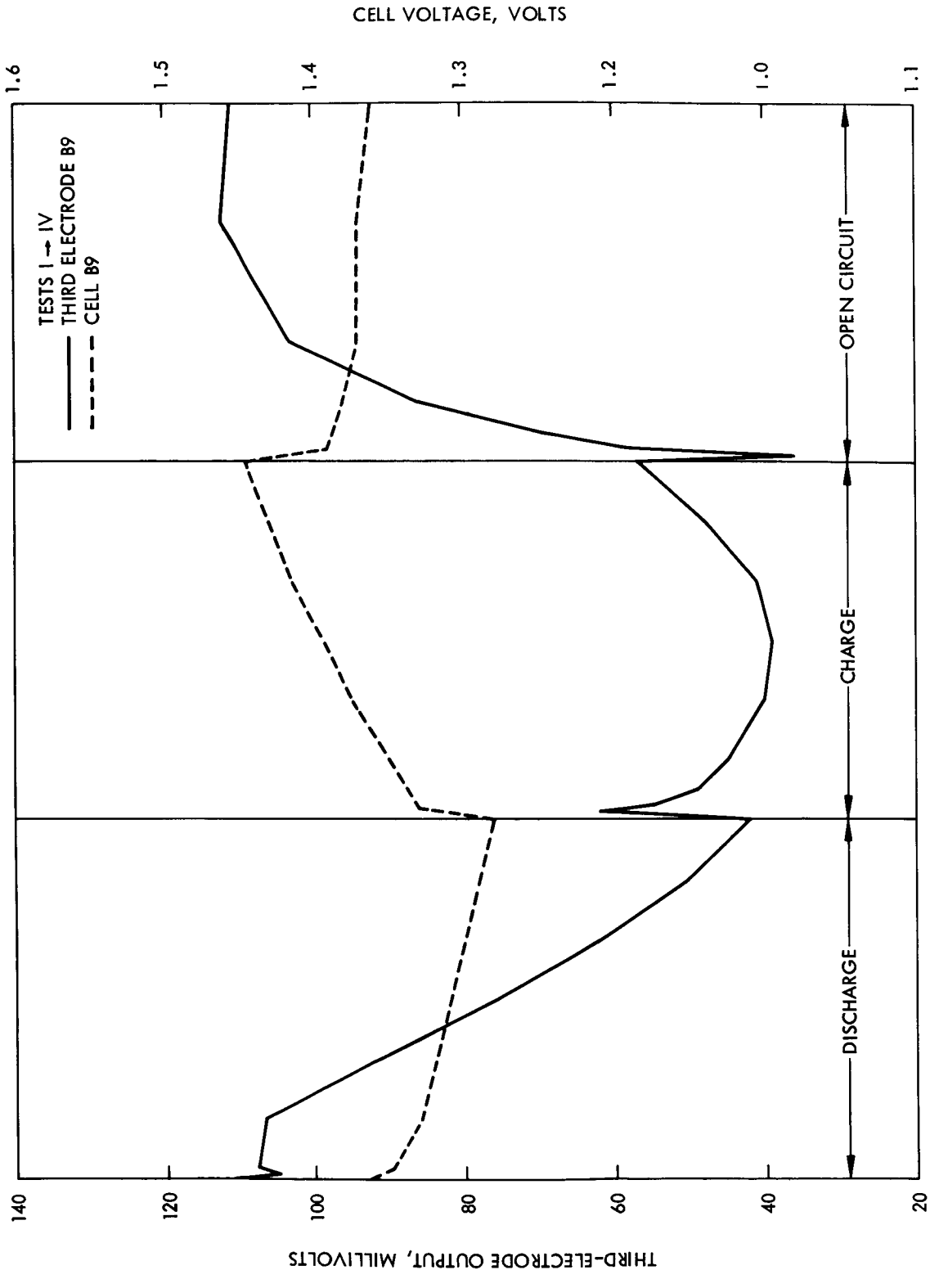


Figure 3-4. Third electrode output and cell voltage versus T, tests I through IV.

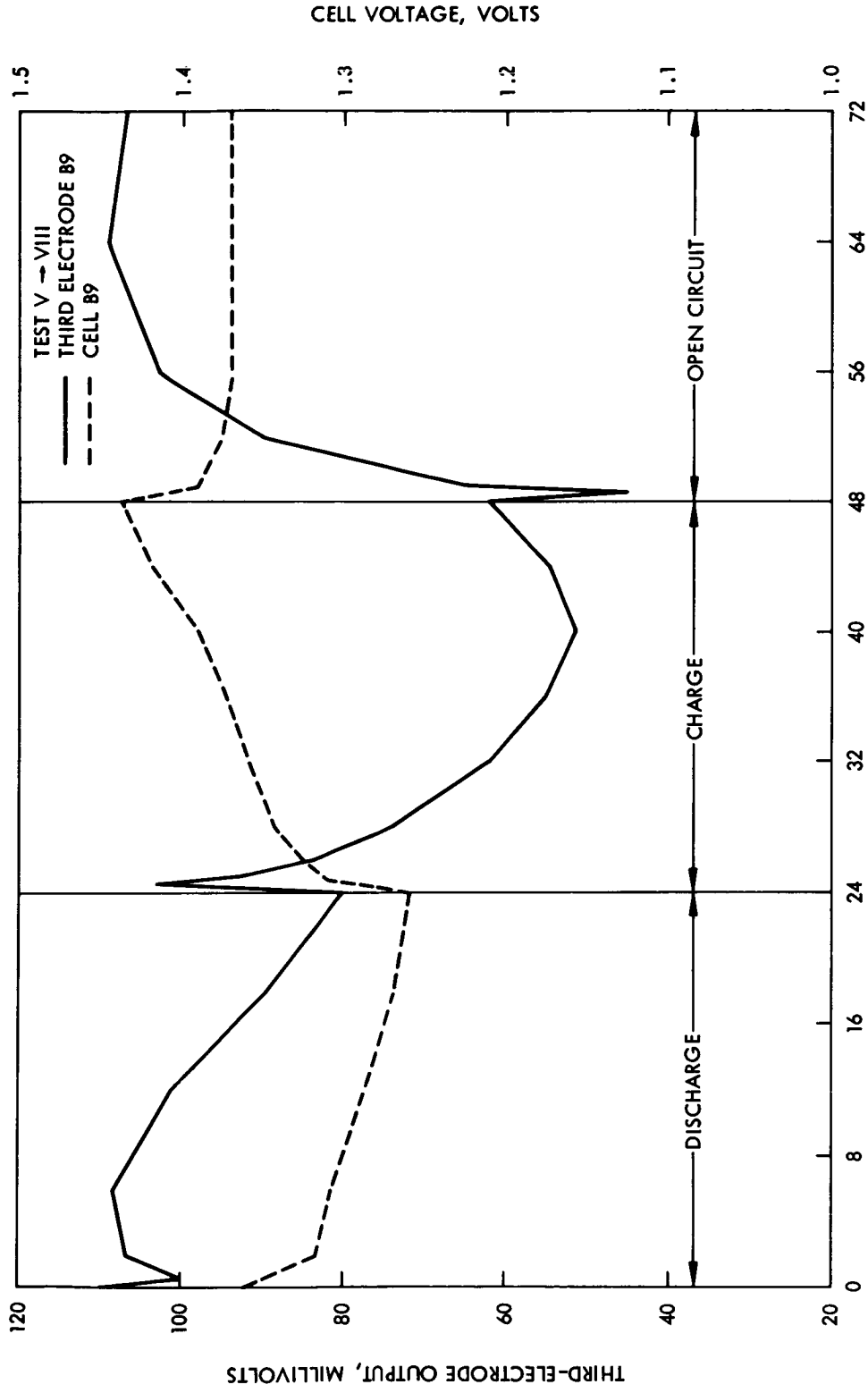


Figure 3-5. Third electrode output and cell voltage versus T, tests V through VIII.

Test No.	Discharge				Charge				Open Circuit Time (Min)
	Rate	Current (Amps)	Depth (%)	Time (Min)	Rate	Current (Amps)	Over Charge (%)	Time (Min)	
1	C/5	2.4	10	30	C/4	3.0	115	27.6	30
2	C/5	2.4	10	30	C/3	4.0	115	20.7	30
3	C/5	2.4	10	30	C/2	6.0	110	13.2	30
4	C/5	2.4	10	30	2C/3	8.0	105	9.4	30
5	C/2	6.0	10	12	C/4	3.0	115	27.6	30
6	C/2	6.0	10	12	C/3	4.0	115	20.7	30
7	C/2	6.0	10	12	C/2	6.0	110	13.2	30
8	C/2	6.0	10	12	2C/3	8.0	105	9.4	30

Table 3-1. Characteristic Test Parameters for Charge-Discharge Cycles

The outputs on Figures 3-4 and 3-5 show a slope difference for the charge-discharge rates, but this difference can be attributed to the difference in the discharge rate that was used for the test cycles. In general, the shape of these curves very closely approximates the curves produced by other sources.

Perhaps the most interesting feature of these curves is the slow response time of the third electrode output to the input changes, from discharge to charge, and to open circuit. The output displays an "electrical inertia," such that when the third electrode begins to respond to an input, it tends to follow that trend for some time after the input is changed, before changing direction to follow the new input.

3.4 CONTROL CIRCUIT DESIGN

For a first attempt to utilize the third electrode output to control the charge of the battery, it seemed most desirable to have some sort of proportional control, such that as the third electrode output approached a predetermined value, the charging current would be appropriately reduced in order to maintain the third electrode output constant at that value. This would permit the battery to charge up to full capacity, and then be held in that condition while the OCR is on. When the OCR turns off (due to low solar panel output), the battery would begin to supply the load from a fully charged condition.

A circuit was designed to perform the desired control, but the slow response of the third electrode output prevented proper operation of the system. As the third electrode output approached a selected level, the charging current was reduced, but the third electrode output continued to rise toward that level. When the third electrode reached the preselected level, the charging current reduced to zero and the OCR turned off. This caused a dip in the output, and the OCR turned back on. The output then went beyond the selected point and the OCR turned off again, which produced another dip in the output. These oscillations continued until the minimum value of the dip in the output was higher than the selected point. At this time the charging current reduced to zero, the OCR turned off, and the battery was forced into a discharge mode to supply the load. The output rose slowly to some peak value and then dropped slowly back toward the selected point. When the output dropped to the selected point, the OCR turned on and began to supply charge to the battery; however, this caused a positive peak in the output which turned off the OCR again. These oscillations continued until the maximum value of the output peak was lower than the control point. The output continued to drop and the charging current increased in an attempt to raise the output level back up to the selected point. When the output level reached some minimum value, it commenced to rise again and the cycle repeated.

While this type of control does work, the battery is subjected to repeated charge-discharge cycles, and this type of operation is deemed unnecessary, and generally detrimental to the overall system.

To eliminate unneccessary discharge of the battery, the system of Figure 3-6 was devised. This technique permits the battery to charge until the third electrode output reaches some predetermined level. At this time, the OCR is turned off, and the bypass switch is turned on, which allows the solar panel to supply the load directly. When the third electrode output drops to some lower level, the OCR is turned back on, and the bypass switch is turned off. The system was designed with this hysteresis to prevent oscillations that occur when the output dips or peaks due to changes in the input to the battery. Note that these dips and peaks are apparent on the curves shown on Figures 3-4 and 3-5. If the solar panel output decreases (due to eclipse or excess cell degradation), or the load requirements increase beyond the capability of the solar panel, the output buss voltage drops. As a result, the diode becomes forward biased and allows the battery to supply the additional current required.

The circuit designed to perform this function is shown schematically in Figure 3-7. This circuit is designed for use with the 250 watt four-phase OCR. The operation of this circuit is as follows. As the third electrode voltage rises to the reference voltage determined by R_5 and R_6, the left side of Q_1 begins to conduct. When the current through the tunnel diode (CR_1) reaches 1 milliamp, the diode flips to its high voltage state and the left side of Q_2 is turned on. When Q_2 is on, the reference side of Q_{13} in the OCR integrator is turned on hard, which causes Q_{14} in the integrator to be turned off. When C_3 charges up, Q_{10} in the peak holding comparator is turned on hard which disables the bistable (Q11 and Q12). With Q14 and the bistable off, the integrator output drops toward -5 volts which turns off the duty factor modulator, and hence turns off the OCR. While this sequence is proceeding, C_4 charges up toward the peak point of Q_3. R14, R15, C4 and Q3 comprise

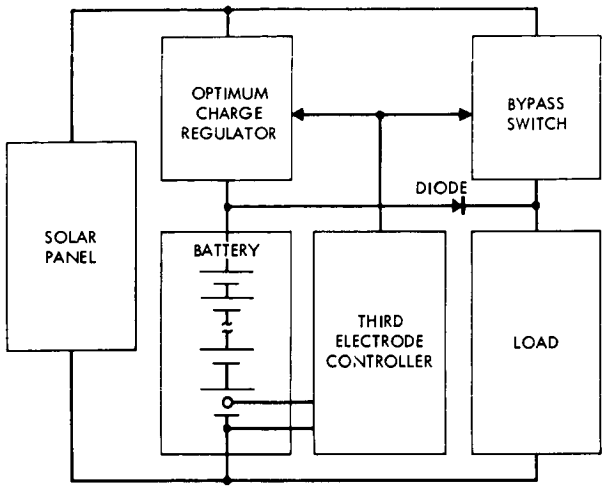


Figure 3-6. Third electrode OCR controller.

a relaxation oscillator which produces a pulse that is applied to the base of Q4. This pulse turns on Q4 (for the duration of the pulse), which turns off Q5, and allows charge to flow through the primary of T_1. This causes the SCR firing pulse to appear across the secondary of T1 (terminals 5 and 6), turning on the SCR. This connects the solar panel to the load. When the pulse ends and Q4 turns off, Q5 turns on permitting charge to flow through the core reset secondary of T1 (terminals 7 and 8). Since the circuit of Q3 is a relaxation oscillator, the pulse output to the SCR is a periodic function, occurring at 5.5 millisecond intervals. The pulse duration is approximately 80 microseconds.

When the third electrode voltage begins to drop, the current through CR_1 decreases, and the voltage at the input base of Q2 decreases. When the current through CR_1 reaches the valley current level (Iv), the diode flips back to its low voltage state, and Q2 turns off. This removes the drive from the pulse generator (Q3) and hence, stops the firing pulses to the SCR. At the same time, the disabling base drive to Q13 is removed and the integrator output rises, turning on the

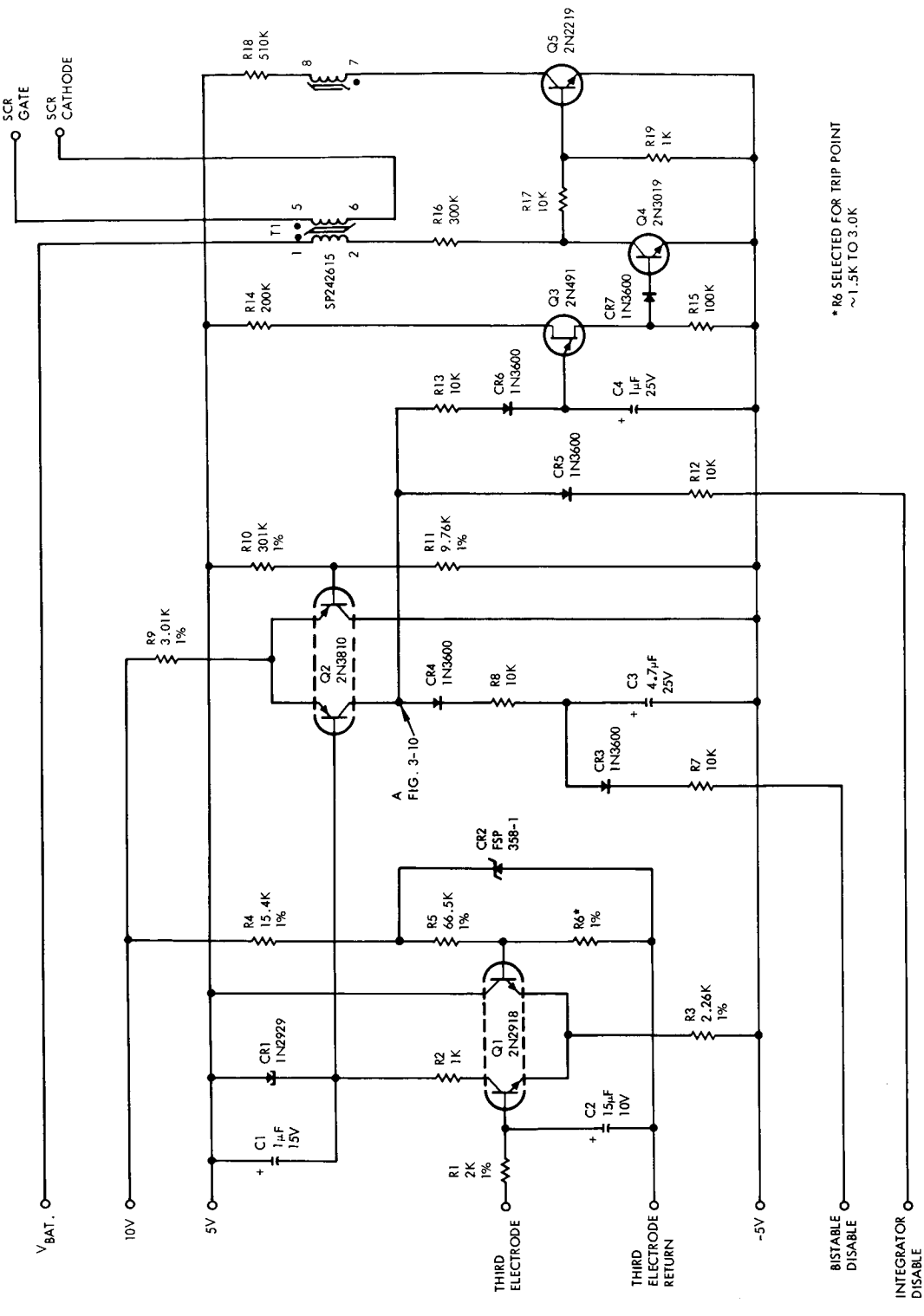


Figure 3-7. Third electrode controller.

duty factor modulator. Due to the charge on C3, the disabling drive to Q10 decays more slowly, and the integrator output continues to rise. This increases the duty factor, and causes the solar panel voltage to drop. The dip in solar panel voltage back biases the SCR, which turns it off. By this time, the disable drive to the bistable has been removed, and the OCR resumes normal operation.

The SCR was chosen as a bypass switch due to the simplicity of the drive circuitry, and the fact that the SCR does not require continuous drive. This results in less power loss in the system, and a higher overall efficiency. There are alternatives to this system, and one such alternate is shown in Figure 3-8. This system has the same front end as the previously described circuit, but instead of driving a relaxation oscillator, the drive is fed to a DC to DC converter which is used to turn on the bypass transistor. This method requires continuous base drive to the transistor; consequently, additional power loss. Diode 2 is also required to prevent possible breakdown of the bypass transistor (base emitter junction) should the solar panel voltage ever drop below the battery voltage.

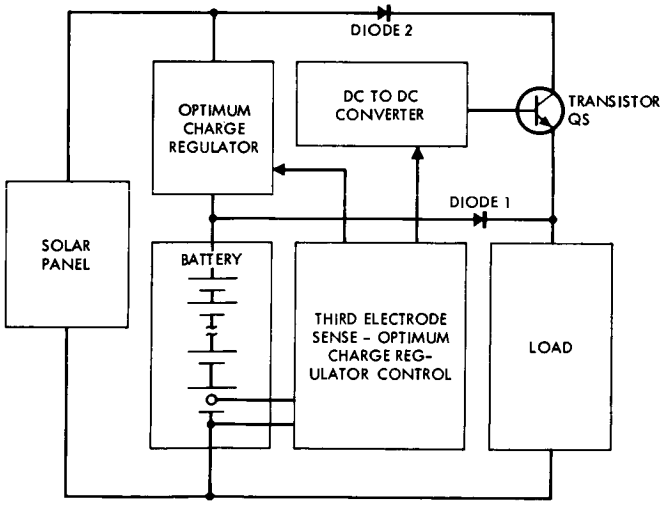


Figure 3-8. Alternate bypass technique.

The third electrode sensing circuit has been shown in its least complicated form, i.e., using only one third electrode, and placing it at the low side of the battery. With slight modifications, this same basic circuit could be used to sense any desired number of third electrode cells. Figure 3-9 shows the block configuration of a system that would sense several third electrodes in a battery. The output of the OR gate is fed to the input of a circuit similar to Q2 in the existing controller configuration (Figure 3-7). The circuit proposed to perform this function is shown in Figure 3-10. This circuit operates in the same manner as the existing circuit described earlier. Beyond point A, the circuit is identical to Figure 3-7 from point A. The major changes are in the positive voltage supplies, the resistors R_E and R_B, and the addition of diode OR gate. The positive voltages are now derived from the battery. The resistors R_E and R_B are chosen to establish the proper references for the particular third electrode cell being sensed. The diode OR gate provides isolation between the sensors, and allows any cell reaching the reference level to operate the controller.

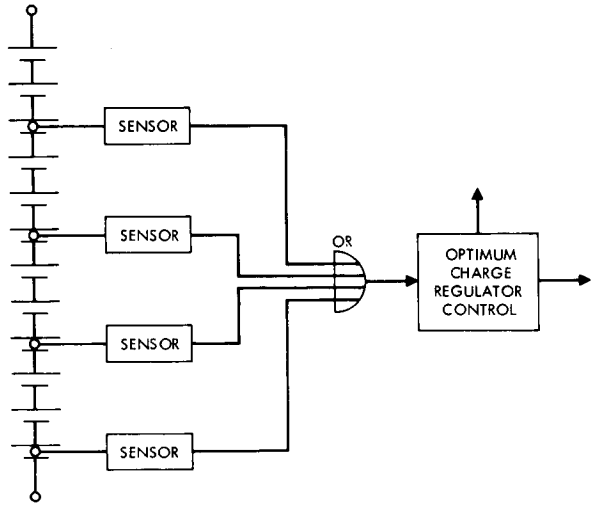


Figure 3-9. Multiple Sensor block diagram.

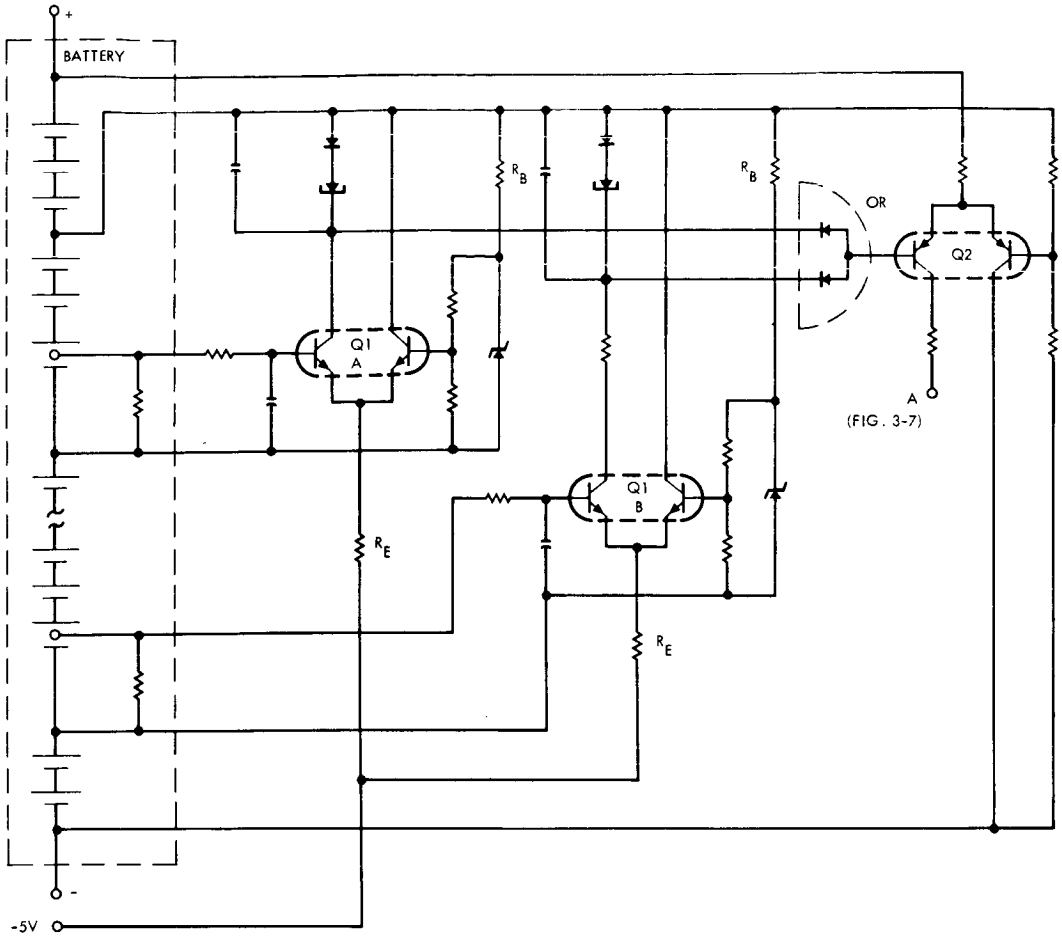


Figure 3-10. Multiple third electrode sensor and gate.

3.5 TESTING WITH THE OCR

After the breadboard circuit for the third electrode controller was fabricated and tested, it was integrated into the system shown in Figure 3-11. The solar panel simulator is connected to the input of the 250 watt four phase OCR. The 27 cell battery (containing three third electrode cells), and a 25 ohm resistive load are connected to the output of the OCR.

The system performed as outlined in the previous section (3.4). Figure 3-12 shows the third electrode output as a function of time for two complete cycles. The time required to "top-off" the battery was approximately 7 minutes at a current of 4.3 Amperes ($\simeq C/2.8$).

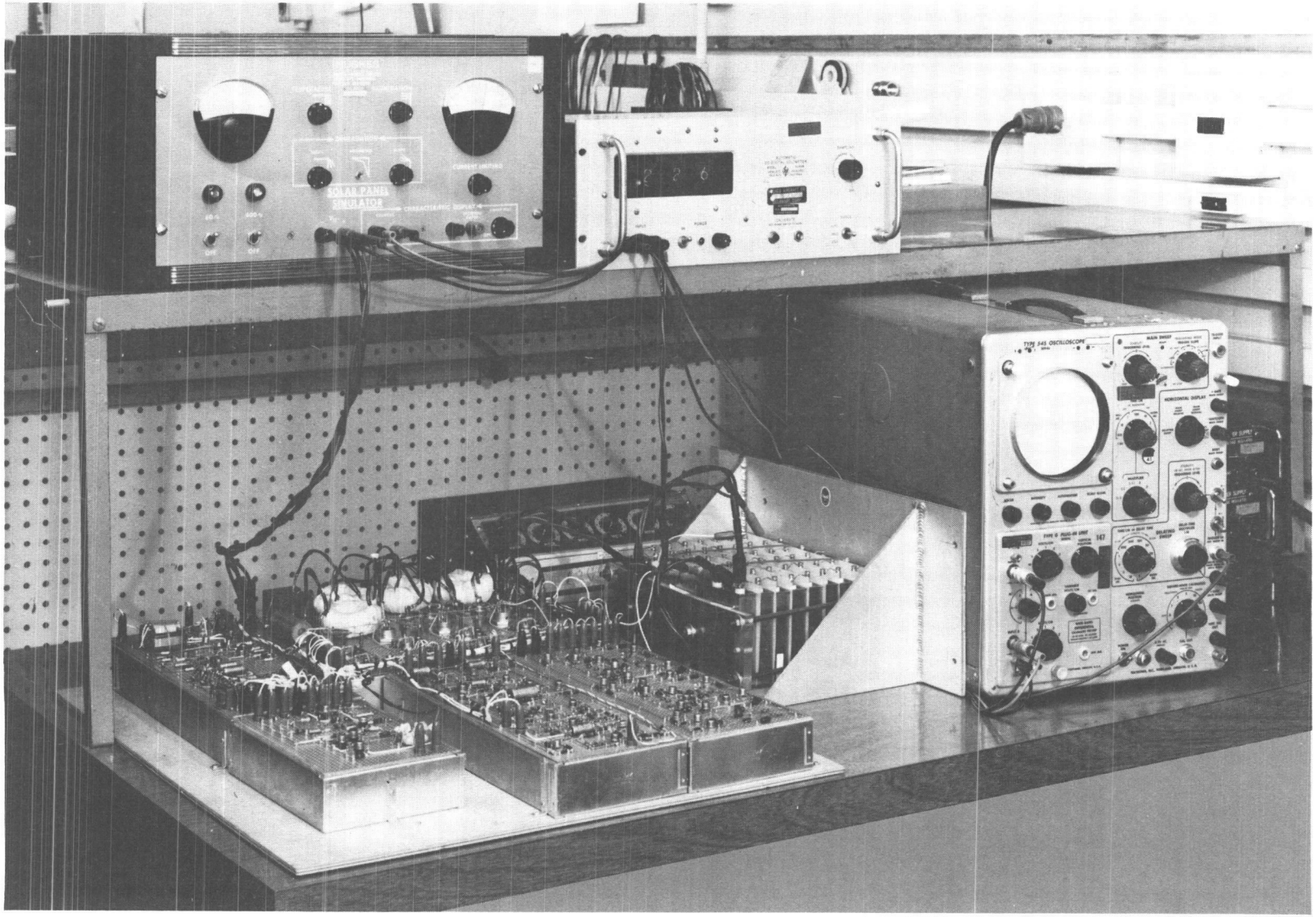


Figure 3-11. 250 watt four phase OCR system.

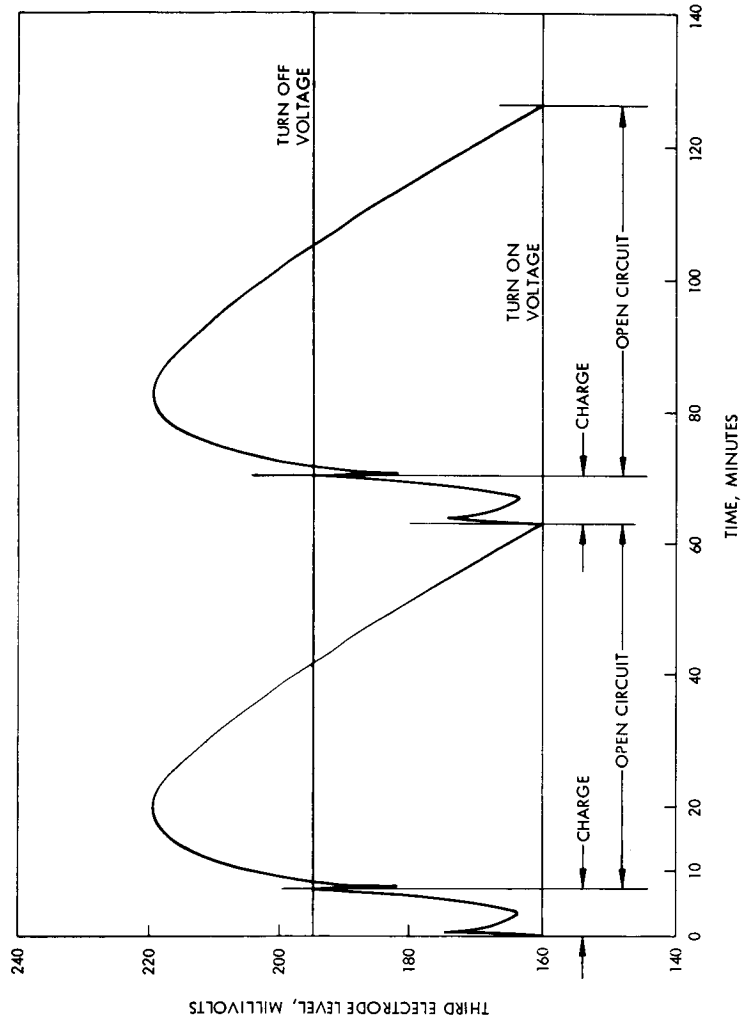


Figure 3-12. Third electrode output using OCR.

The open circuit time was approximately 56 minutes, and the time for one complete cycle was 63 minutes. The lower (turn on) limit was 160 millivolts, and the upper (turn off) limit was 195 millivolts, giving a hysteresis of 35 millivolts. The curves show the overshoot, or electrical inertia described earlier.

The output to the SCR is shown as the upper trace of Figures 3-13 and 3-14. The lower trace shows the voltage change across Q4 (ce). Figure 3-13 shows that the interval between pulses is 5.5 milliseconds and the pulse amplitude is approximately three (3) volts. The small negative going pulse following the firing pulse is caused by the reset current through winding 7 and 8. Figure 3-14 shows that the duration of the firing pulse is 80 microseconds. Figure 3-15 shows the output of the reset secondary (winding 7 and 8) as the upper trace, and the voltage across Q_4 as the lower trace. This indicates that the reset time for the core is approximately 350 microseconds.

3.6 SUMMARY

In general, it does seem feasible to utilize the third electrode output to control the OCR. The slow response time of the third electrode does seem to preclude any form of proportional control; however, the designs presented here use this slow response to an advantage. When several third electrode cells are used to establish control, the system becomes more cumbersome in parts count, but yields a higher reliability due to the inherent redundancy. The SCR switch provides a simple, low loss means of bypass when the battery becomes fully charged. Other methods of bypass are possible, but these require greater power expenditure. Therefore, the SCR was chosen as the most desirable technique.

Upper: 2 V/cm

Lower: 20 V/cm

Horiz: 1 millisec/cm

Upper: Output to SCR

Lower: Q4 Vce

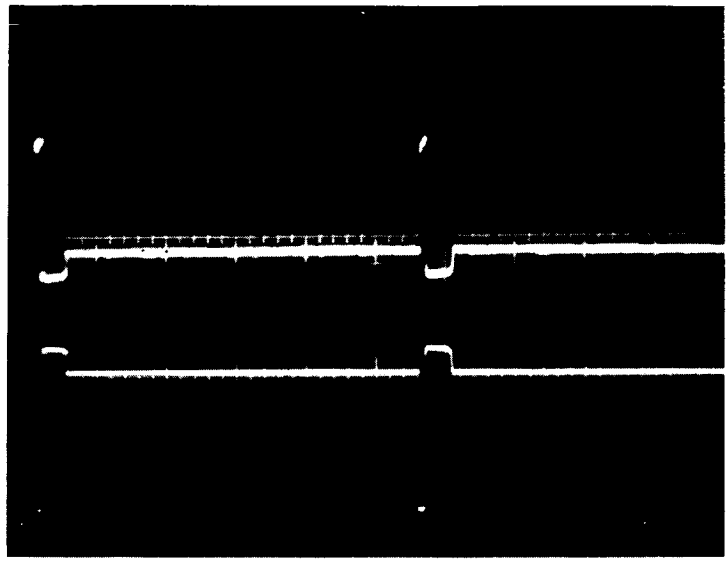


Figure 3-13. SCR firing pulse.

Upper: 2 V/cm

Lower: 20 V/cm

Horiz: 10μsec/cm

Upper: Output to SCR

Lower: Q4 Vce

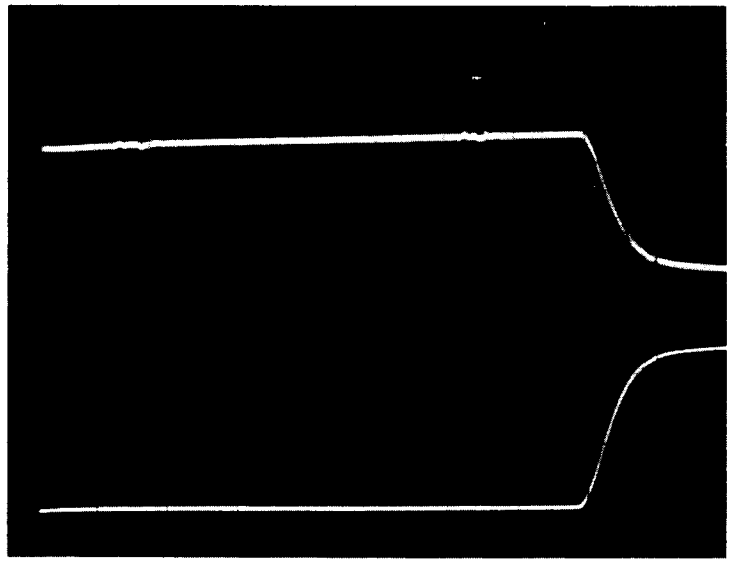
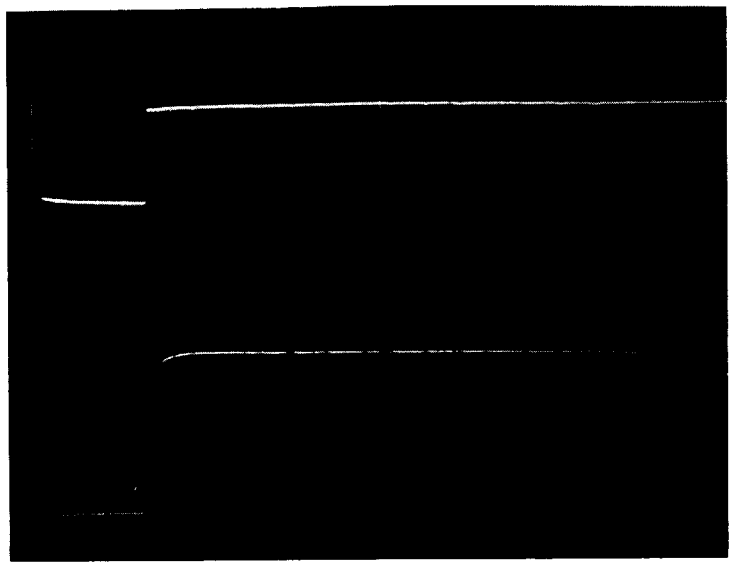


Figure 3-14. SCR firing pulse.



Upper trace: Terminal 7 and +5$\frac{V}{-}$ buss. 5$\frac{V}{-}$/cm.
Lower trace: Vce of Q4 20$\frac{V}{-}$/cm.
Horiz : 50μsec/cm.

Figure 3-15. Core reset pulse.

4. FAILURE MODE ANALYSIS AND MULTIPHASE OPERATION

The results of the failure mode analysis performed on the OCR are given in Table 4-1 as a Mean Time Between Failure (MTBF) figure. This MTBF is obtained by taking the reciprocal of the failure-rate summation. The failure-rate of all electrical components were obtained directly from MIL-HDBK 217A with the exceptions of transformers and chokes. These represent operational space data taken from Hughes Systems.

The failure-rates obtained from MIL-HDBK 217A will reflect a more pessimistic figure than if failure-rates used in space programs were used. This is due to the higher reliability achieved by the stringent screening of space parts. The transformers and chokes were designed by Hughes so the failure-rate from Hughes Systems would be more applicable.

Parts failure is primarily caused by electrical stress, thermal stress and mechanical stress. However, for well designed equipment, the principle stress factors are electrical and thermal. The other factors contributes only second order effects.

In determining the parts failure-rate, the stress ratio as required by MIL-HDBK 217A is calculated by dividing the nominal operating stress by the rated stress. For example, the stress ratio of a resistor is $\frac{\text{"nominal operating wattage"}}{\text{rated wattage}}$, and of a capacitor is $\frac{\text{"nominal operating voltage"}}{\text{rated voltage}}$. In determining the thermal stress, "hot-spots" were ignored and an ambient temperature of +25 °C was used. For stud-mounded devices, a case temperature of +100 °C was used to simplify calculation.

The component part failure modes required for the MTBF calculation were obtained from Hughes Components Application and Reliability Handbook for Aerospace Equipment and are summarized in Table 4-2.

	Parts Counts Prediction λ (Failure/10^6 Hours)	Failure Mode Analysis λ (Failure/10^6 Hours)
250 Watt OCR		
Switching Circuit	23.46	10.83
Duty Factor Modulator	14.84	8.58
Switching Regulator & Bias Converter	10.64	8.57
Current Sensing Amplifier, Peak Holding Comparator, Bistable & Integrator	13.98	8.74
Total Failure Rate (λ)	62.92	36.72
MTBF ($\frac{1}{\lambda}$)	15,900 Hours	27,200 Hours
50 Watt OCR		
Switching Circuit	13.90	9.66
Duty Factor Modulator	7.28	5.72
Switching Regulator & Bias Converter	10.55	8.83
Current Sensing Amplifier, Peak Holding Comparator, Bistable & Integrator	12.32	7.44
Total Failure Rate (λ)	44.05	31.65
MTBF ($\frac{1}{\lambda}$)	22,700 Hours	31,700 Hours

Table 4-1. Failure rate summary.

Part Type	Catastrophic Failure Mode (% Occurrence)	
	Short	Open
Capacitors		
Paper (Dielectric)	80	20
Dipped Mica (Dielectric)	90	10
Solid Tantalum, polarized	90	10
Glass (Dielectric)	90	10
Resistors		
Fixed Carbon Composition	90	10
Metal (Carbon) Film	10	90
Power Wirewound	10	90
Transistors	90	10
Diodes	90	10
Transformers	60	40
Chokes and Coils	10	90

Table 4-2. Component part failure modes.

The result of the failure mode analysis (The MTBF) based on a parts count prediction is 15,900 hours for the 250 watt OCR and 22,700 hours for the 50 watt OCR. The MTBF based on the failure mode analysis is 27,200 hours for the 250 watt OCR and 31,700 hours for the 50 watt OCR.

The MTBF based on the failure mode analysis is obtained by multiplying the failure-rate by a weighting factor ranging from 0 to 1. The value of this factor depends upon what happens to the equipment when a catastrophic failure of any individual part occurs.

A failure-rate summary and a reliability block diagram are shown on Table 4-1 and Figure 4-1 respectively.

The MTBF based on the failure mode analysis is approximately twice the MTBF based on parts count for the 250 watt OCR. This ratio is 1.4 for the 50 watt OCR. The higher ratio for the 250 watt OCR is due to the fact that it is a four phase OCR as compared to two phase,

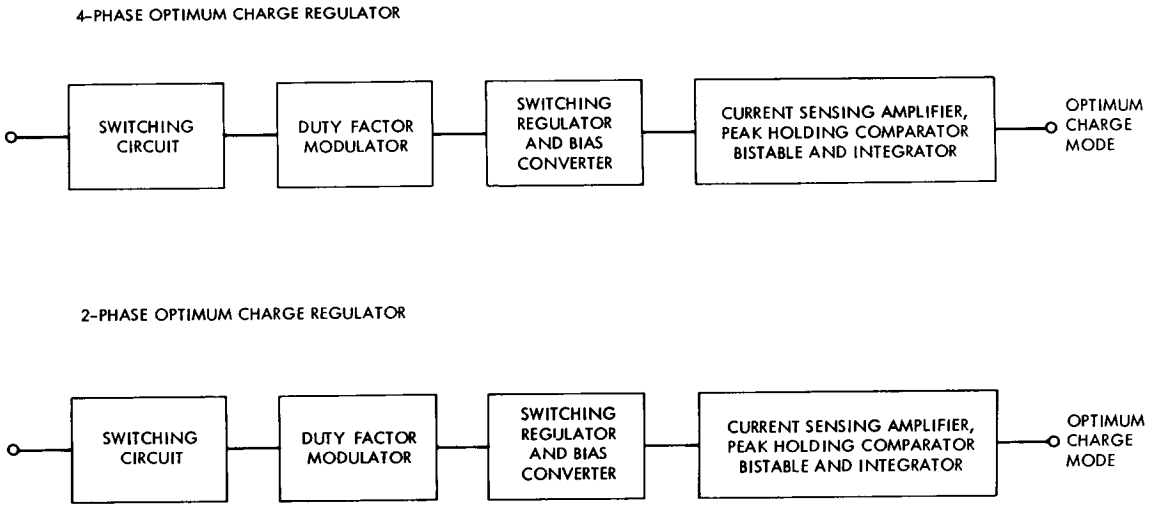


Figure 4-1. OCR – reliability block diagram.

50 watt OCR. This permits one phase of the four phase OCR to be disabled without any appreciable decrease in efficiency. This is not true with the two phase OCR.

Although there are more parts in the 250 watt OCR as compared to the 50 watt OCR, its MTBF based on the failure mode analysis is 27,200 hours as compared to 31,700 hours for the 50 watt OCR; a decrease of 14%. In return the 250 watt OCR has five times the power transfer capability plus a slightly higher efficiency.

4.1 MULTIPHASE OPERATION

To insure operation of a multiphase OCR in the event that one phase fails, some circuit modifications are required.

First consider the 50-watt, two phase regulator, and assume that one phase is rendered inoperative in such a manner that the remaining phase can still function. (Note: this mode of failure will occur if the switching transistor or the inductor primary are open, or if no base drive can be applied to the switching transistor.) The current sense amplifier detects the power decrease due to the missing phase, and in turn the integrator output increases. This causes the duty factor to the remaining phase to increase in order to restore the power level to the optimum region. The energy through the operative phase is doubled, and consequently several components bear the increased current and power levels. Since the energy requirement through the phase has now doubled, the current increases by a factor of $\sqrt{2}$, from

$$E = 1/2\ L\ I^2 = 1/2\ L\ p\left(\frac{V_{sp}}{Lp} D_1\ T\right)^2$$

The base drive to the switching transistor must be increased by a factor of $\sqrt{2}$, and the inductance in the switching transformer must be lower. In essence, this requires that each phase be designed to operate as a single phase circuit; however, several factors must be examined to determine the advisability of these modifications.

In the case of the 250 watt four phase OCR, the energy requirement through each phase increases by a factor of 1.3. Hence, the current increase is only $\sqrt{1.3}$ times as great, or approximately 1.14. This increase in current and power handling capability requires fewer changes than those necessary with the two phase OCR. It becomes apparent that as the number of phases is increased, fewer circuit modifications are required to insure operation with one phase disabled.

5. OPTIMUM CHARGE REGULATOR WORST CASE AND STRESS ANALYSIS

A worst-case analysis was performed on the optimum charge regulator (OCR) to determine whether normal operation would occur under worst case solar panel, battery, temperature, component parameter, and aging variations.

The charge regulator was divided into blocks, as shown in Figure 5.0-1, to facilitate analysis. Critical input and output parameters were defined for each block, beyond which the circuit would not function properly. These were used as the limits for worst-case consideration. Equivalent circuits and mathematical models were derived when required. If a block was deemed unsatisfactory under worst case conditions, corrective design changes were suggested.

Analysis was performed on the OCR by using the following worst-case design parameters:

1. Minimum temperature = -40°C
   Maximum temperature = +70°C
2. 1 percent resistors vary ±5 percent
   5 percent resistors vary ±20 percent
3. Tantalum capacitors vary ±20 percent
   Paper capacitors vary ±5 percent
4. Bias supply voltages vary ±0.1 volts

A stress analysis was performed on each block to insure that all components were adequately derated. The maximum allowed derating factor (the ratio of operating voltage, current, or power to rated voltage, current, or power) for all components were as follows:

Component Type	Derating	Parameter
1) Resistors	50 percent	Power
2) Capacitors	70 percent	Voltage
3) Diodes	50 percent	Peak inverse voltage
	50 percent	Current
4) Transistors	50 percent	Vceo
	50 percent	Power

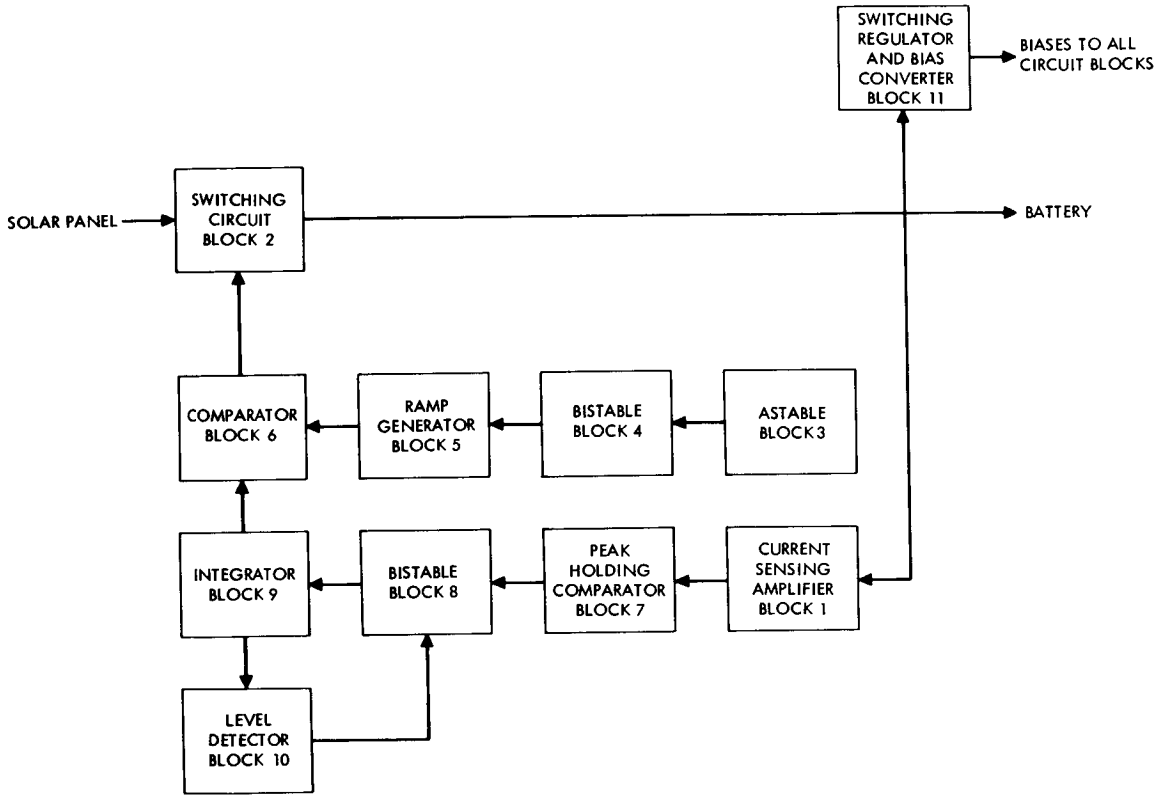


Figure 5.0-1. Optimum charge regulator block diagram.

Two optimum charge regulators have been designed: a 250-watt four-phase regulator and a 50-watt two-phase regulator. Since designs of both regulators are similar, corresponding blocks as shown in Figure 5.0-1 are analyzed together. Analysis is carried out according to block number.

5.1 BLOCK 1, CURRENT SENSING AMPLIFIER

The current sensing amplifier consists of a high gain amplifier with feedback as shown in Figure 5.1-1 and Figure 5.1-2. Worst-case analysis was performed by developing an equivalent circuit model of Figure 5.1-1. From the model a general transfer function was derived. Computer programs were written to solve for gain versus frequency response. The BASIC language system was used and the programs were processed on a GE 265 time sharing computer. Theoretical results were compared with a measured response to determine the validity of the derived transfer function. Worst-case parameters at both temperature extremes (-40°C and +70°C) were then used to obtain worst-case responses.

Experiments have shown that the midband gain can vary at least ±10 db from the nominal 60 db without hindering system operation. These criteria were set as worst-case limits.

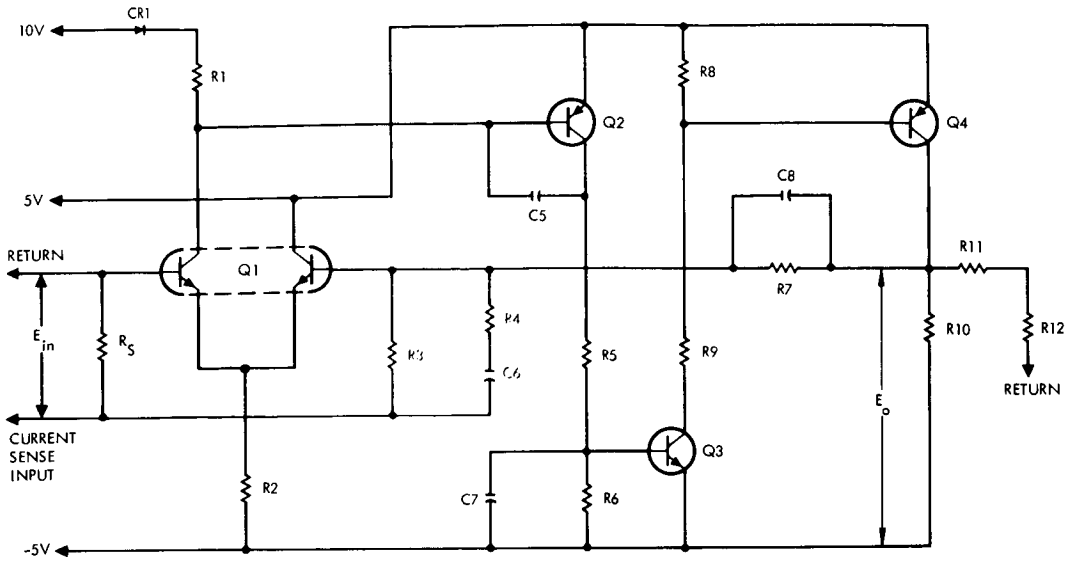
5.1.1 Equivalent Circuit Model

The low frequency model is used since the frequency range of interest is zero to ten kHz. This is considerably lower than the gain cutoff frequency of any of the transistors in the circuit.

Transistors Q_2, Q_3, and Q_4 (Figure 5.1-1) have the equivalent circuit as shown in Figure 5.1-3.

A model for the differential amplifier, Q_1, (Figure 5.1-1) is shown in Figure 5.1-4.

Referring to Figure 5.1-1 and the equivalent circuits of Figures 5.1-3 and 5.1-4, the open loop equivalent circuit can be drawn as shown in Figure 5.1-5.



NOMINAL CIRCUIT VALUES

R1 = 49.9K	R5 = 10K	R9 = 1K	C5 = 0.01 μF	Q1 = 2N2918
R2 = 22.1K, 1%	R6 = 10K	R10 = 2K	C6 = 10 μF	Q2 = 2N1132
R3 = 7.2K	R7 = 51K	R11 = 100	C7 = 1 μF	Q3 = 2N2219
R4 = 100	R8 = 10K	R12 = 510	C8 = 4.7 X 10^{-3} μF	Q4 = 2N1132

Figure 5.1-1. Current sensing amplifier.

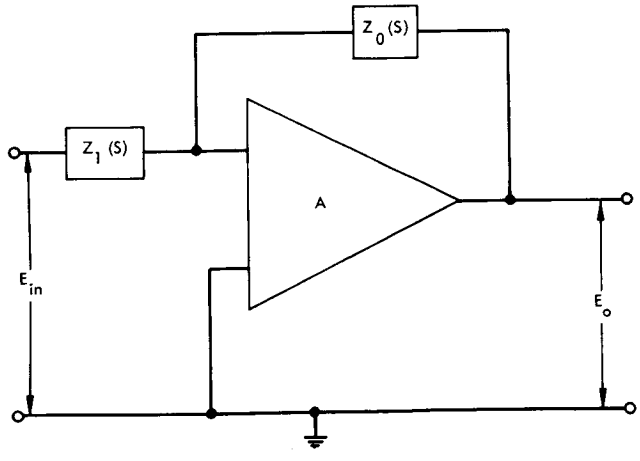


Figure 5.1-2. Current sensing amplifier model.

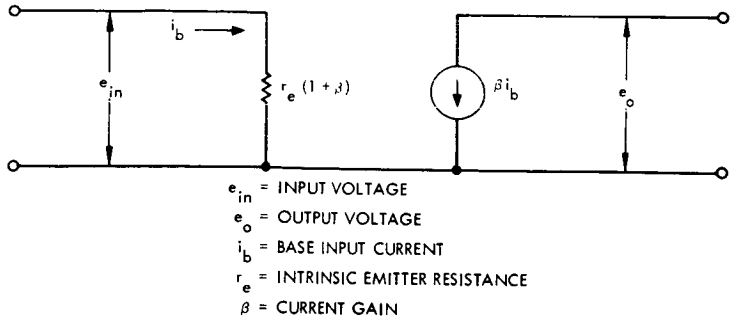


Figure 5.1-3. Common emitter transistor model.

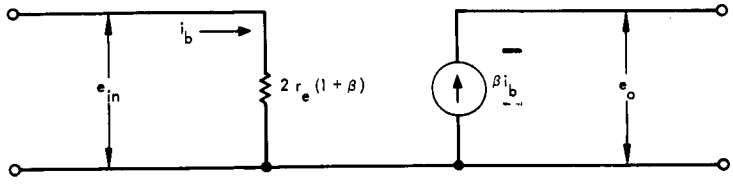
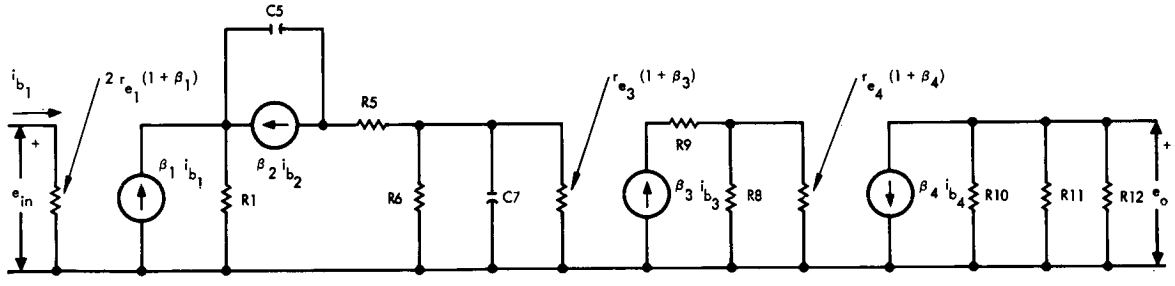


Figure 5.1-4. Differential amplifier model.



SUBSCRIPTS ON β, r_e AND i_b REFER TO THE TRANSISTOR SIMILARLY SUBSCRIPTED. (EG. i_{b_3} IS BASE CURRENT FOR Q3)

Figure 5.1-5. Open loop equivalent circuit.

5.1.2 Transfer Function

Figure 5.1-2 is the general configuration of the current sensing amplifier. It can be shown that the transfer function, $\frac{E_o}{E_{in}}$, is the following:

$$\frac{E_o}{E_{in}} = - \frac{AZ_o(s)}{Z_o(s) + Z_1(s) + AZ_1(s)} \qquad (5.1\text{-}1)$$

where

A = open loop transfer function

$Z_1(s)$ = input impedance transfer function (R_3, R_4, and C_6 of Figure 5.1-1)

$Z_o(s)$ = feedback impedance transfer function (C_8 and R_7 of Figure 5.1-1)

The open loop transfer function, A, was developed from Figure 5.1-5 and gave the following result:

$$A = \frac{e_o}{e_{in}}$$

$$= - \frac{\beta_4 R_p R_8 \beta_3 R_1 \beta_1 Z_A (sC_5 r_{e_2}(1 + \beta_2) - \beta_2)}{2(r_4 + R_8) r_1 r_3 [(1 + sC_5 Z)(sC_5 R_1 r_{e_2}(1+\beta_2) + r_{e_2}(1+\beta_2) + R_1) - R_1(sC_5 r_{e_2}(1+\beta_2) - \beta_2) sC_5]} \qquad (5.1\text{-}2)$$

where

$$R_p = R_{10} \,||\, R_{11} \,||\, R_{12}$$

$$Z = R_5 + \frac{R_6 r_3}{R_6 + r_3 + R_6 r_3 sC_7} \qquad (5.1\text{-}3)$$

$$Z_A = \frac{R_6 r_3}{R_6 + r_3 + R_6 r_3 sC_7} \qquad (5.1\text{-}4)$$

$Z_1(s)$ is R_3 in parallel with R_4 and C_6.

$$Z_1(s) = \frac{R_3 + R_4 R_3 sC_6}{sC_6[R_3 + R_4] + 1} \qquad (5.1\text{-}5)$$

$Z_o(s)$ is C_8 in parallel with R_7.

$$Z_o(s) = \frac{R_7}{1 + sC_8 R_7} \qquad (5.1\text{-}6)$$

Eq. (5.1-2) to Eq. (5.1-6) may be substituted into Eq. (5.1-1) to yield the closed loop transfer function $\frac{E_o}{E_{in}}$.

5.1.3 Graphical Results

When the nominal component parameters were substituted into the closed loop transfer function, the curve of Figure 5.1-6 was obtained. Nominal values for capacitors and resistors were used. The transistor current gains (β) were measured at their nominal operating currents and these values were used for the actual calculation.

The gain versus frequency characteristic of the amplifier was measured under laboratory conditions. The results of this test are also shown in Figure 5.1-6. As can be seen in this figure, there is a close correlation between the measured and the calculated response.

Worst-case low temperature response was determined by choosing component values such that overall voltage gain was minimized. Figure 5.1-7 compares worst-case response at low temperature, with the nominally calculated values. Figure 5.1-8 compares worst case response at high temperature with the nominal. The component values for this case were chosen to maximize the gain. Gain at midband only varies ±5 db from nominal gain of 60 db for the worst-case conditions. Since this variation is within the limits of the original criterion of ±10 db, it can be concluded that the current sensing amplifier will perform satisfactorily under the worst-case conditions.

5.1.4 Stress Analysis

The electrical stress analysis on all the components of the current sensing amplifier was completed. Results of this analysis are shown in Table 5.1-1.

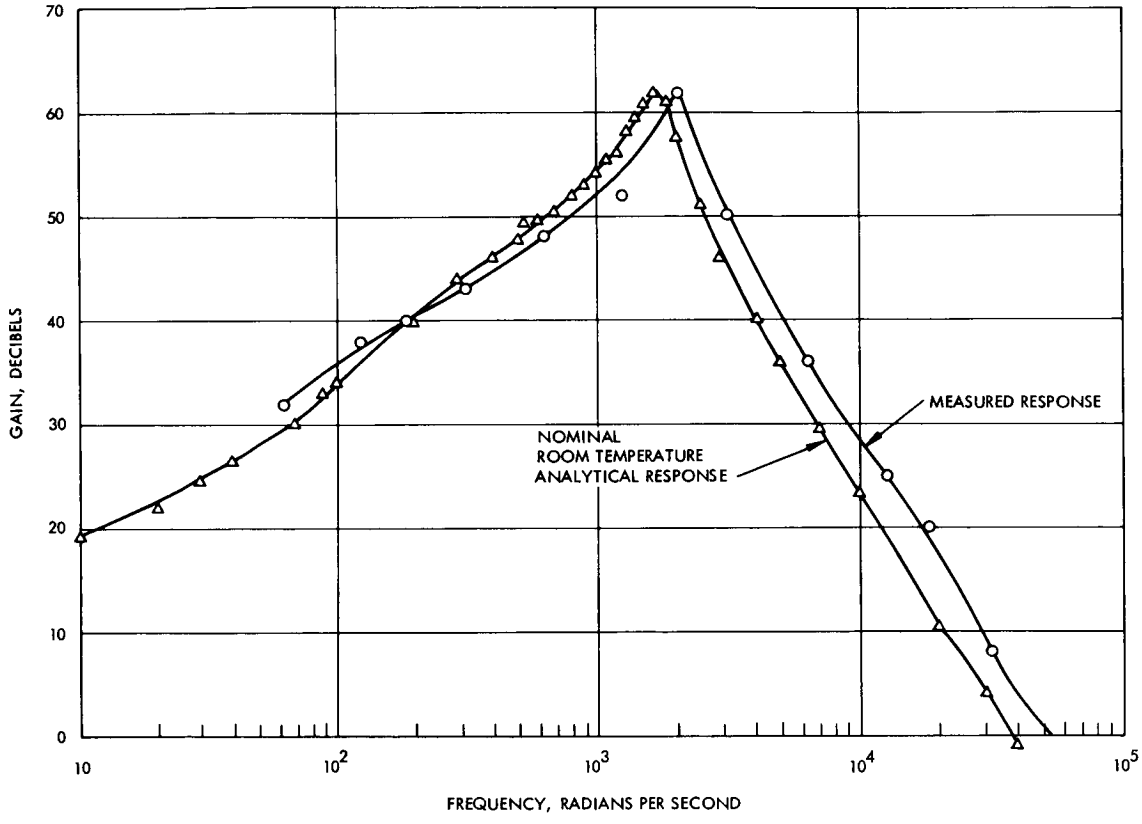


Figure 5.1-6. Gain versus frequency, measured and analytical response.

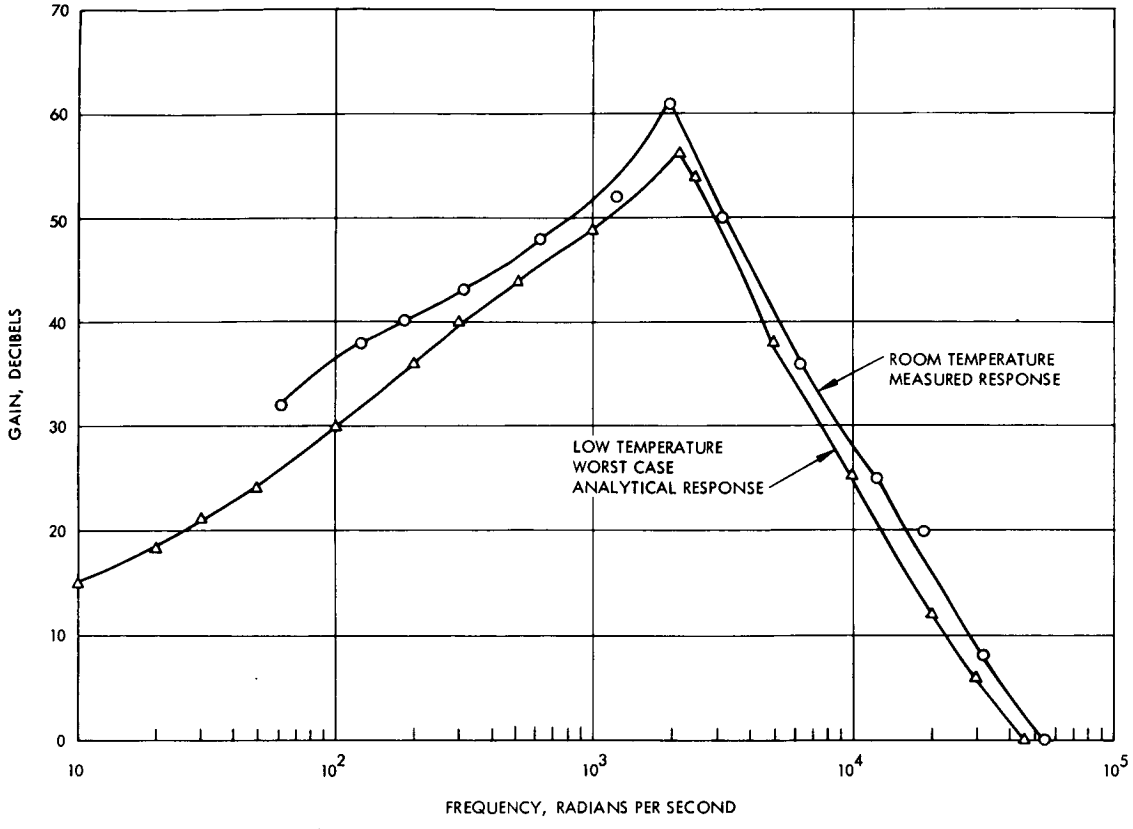


Figure 5.1-7. Low temperature worst-case response.

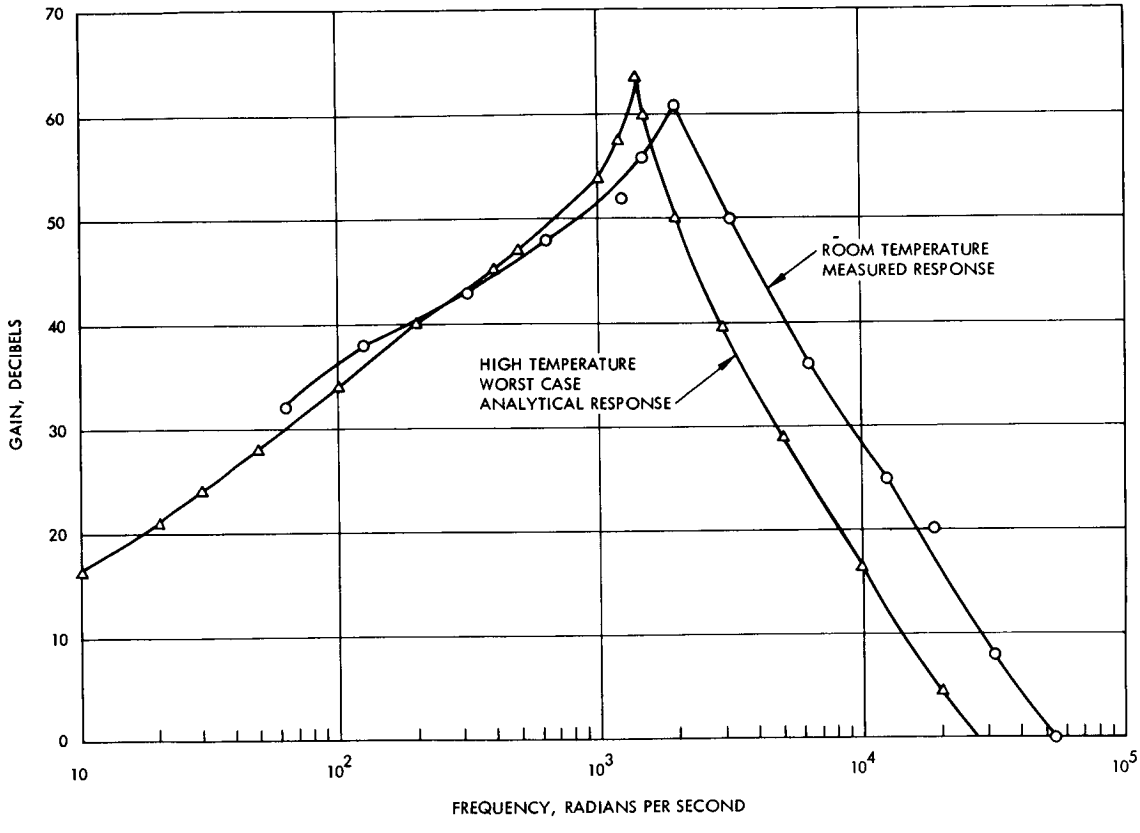


Figure 5.1-8. High temperature worst-case response.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation mw*			Power Dissipation mw*		
Transistors			Vceo (volts)			Vceo (volts)	
Q_1	2N2918	300	45		<1	5	
Q_2	2N1132	1 watt	35		<1	10	
Q_3	2N2219	800	40		1	10	
Q_4	2N1132	1 watt	35		63	10	
Resistors							
R_1	49.9K	250			<1		
R_2	22.1K	125			1		
R_3	7.2K	250			<1		
R_4	100	250			<1		
R_5	10K	250			<1		
R_6	10K	250			<1		
R_7	51K	250			<1		
R_8	10K	250			<1		
R_9	1K	250			<1		
R_{10}	2K	250			13		
R_{11}	100	250			60		
R_{12}	510	250			32		
Capacitors	μf		(volts)			(volts)	
C_5	.01		100			15	
C_6	10		20			1	
C_7	1		20			1	
C_8	4.7×10^{-3}		100			5	
Diodes			PIV (volts)	I_f (ma)		PIV (volts)	I_f (ma)
CR_1	1N3600	500	50	200	<1	0	.1

*Unless otherwise noted.

Table 5.1-1. Stress analysis summary for block 1.

5.2 BLOCK 2, SWITCHING CIRCUIT

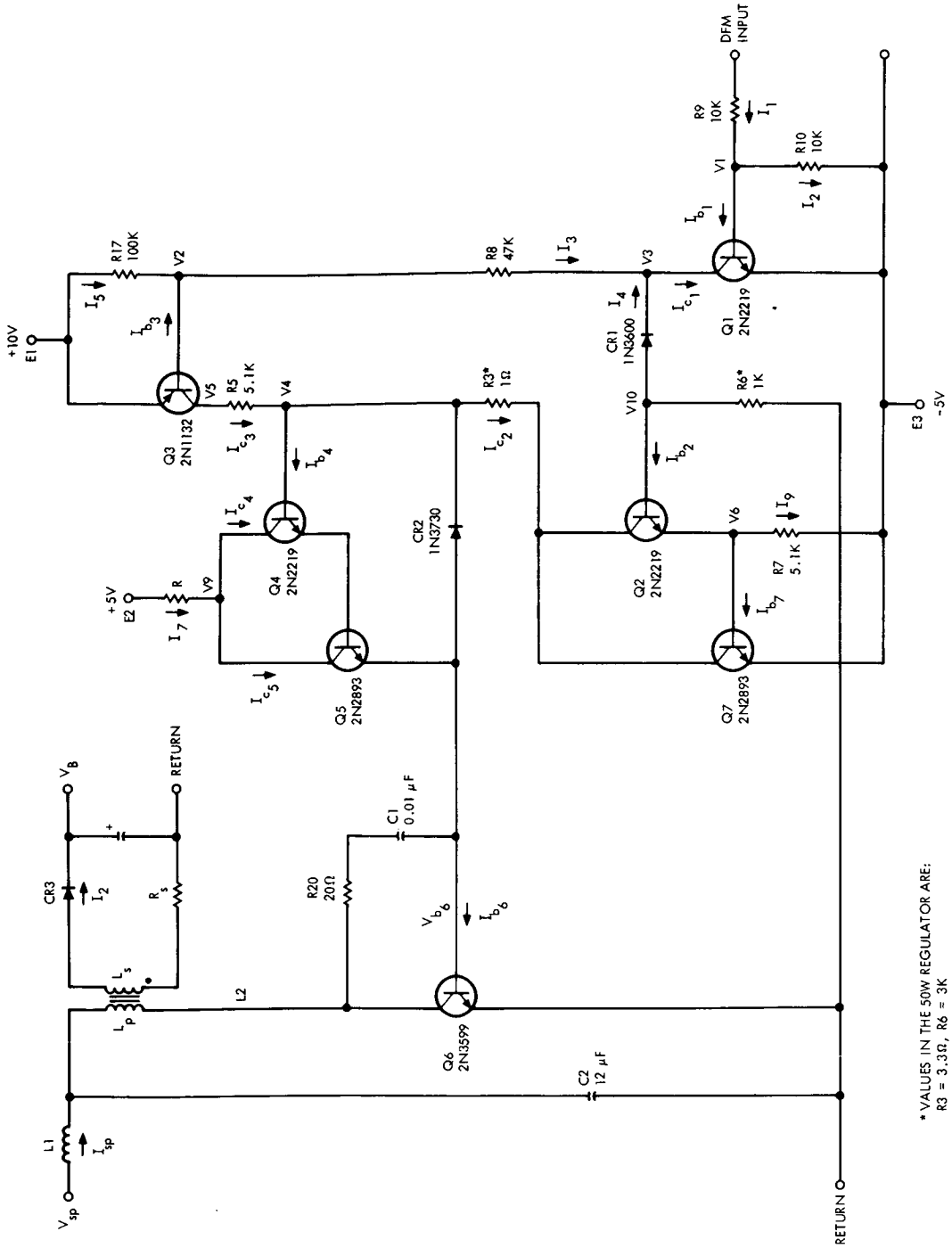
In terms of overall system efficiency, this circuit plays the most important part. Its function is to transfer the power from the solar panel to the battery. A schematic diagram of the entire switching circuit is shown in Figure 5.2-1.

The operation of this circuit proceeds as follows. If at t = 0, the duty factor modulator (DFM) input goes from -5 volts to +5 volts as shown in Figure 5.2-2a, then this signal will be amplified by the succeeding stages, thereby allowing Q_6 to turn "on". As shown by the waveform of Figure 5.2-2b, the collector-emitter voltage of Q_6 will go from V_{sp} to V_{ce_6} (sat) and the current in L_p will begin increasing linearly as shown in Figure 5.2-2c. At time τ_1, the duty factor modulator input returns to -5 volts. This allows Q_7 to turn "on", thereby reverse biasing Q_6 and turning it "off". During the "on" time of Q_6, CR_3 is reverse biased. When Q_6 turns "off", the voltage across the secondary of L2 increases until it forward biases CR_3 and begins delivering current to the battery. This current is a linearly decreasing ramp as shown in Figure 5.2-2d. During the time that I_2 is flowing, the battery voltage divided by the turns ratio is impressed across the primary of the choke. When I_2 ceases to flow at τ_2, the voltage across L_p drops to zero and therefore the collector voltage of Q_6 drops to V_{sp}. The circuit is now ready to begin the cycle anew at time T.

5.2.1 Worst-Case Analysis

A worst-case analysis is performed on the switching circuit to determine if Q_6 will turn "on" and "off" under worst-case input component variations. The 250 watt OCR is considered first. Then the 50 watt OCR is examined.

Switching transistors are saturated if the maximum forced current gain (beta), βf_{max}, is less than the minimum beta of the transistor. Forced beta is equal to maximum collector current divided by the minimum base current. "Off" conditions occur when the base current is defined to be zero.



*VALUES IN THE 50W REGULATOR ARE:
R3 = 3.3Ω, R6 = 3K

Figure 5.2-1. Switching circuit.

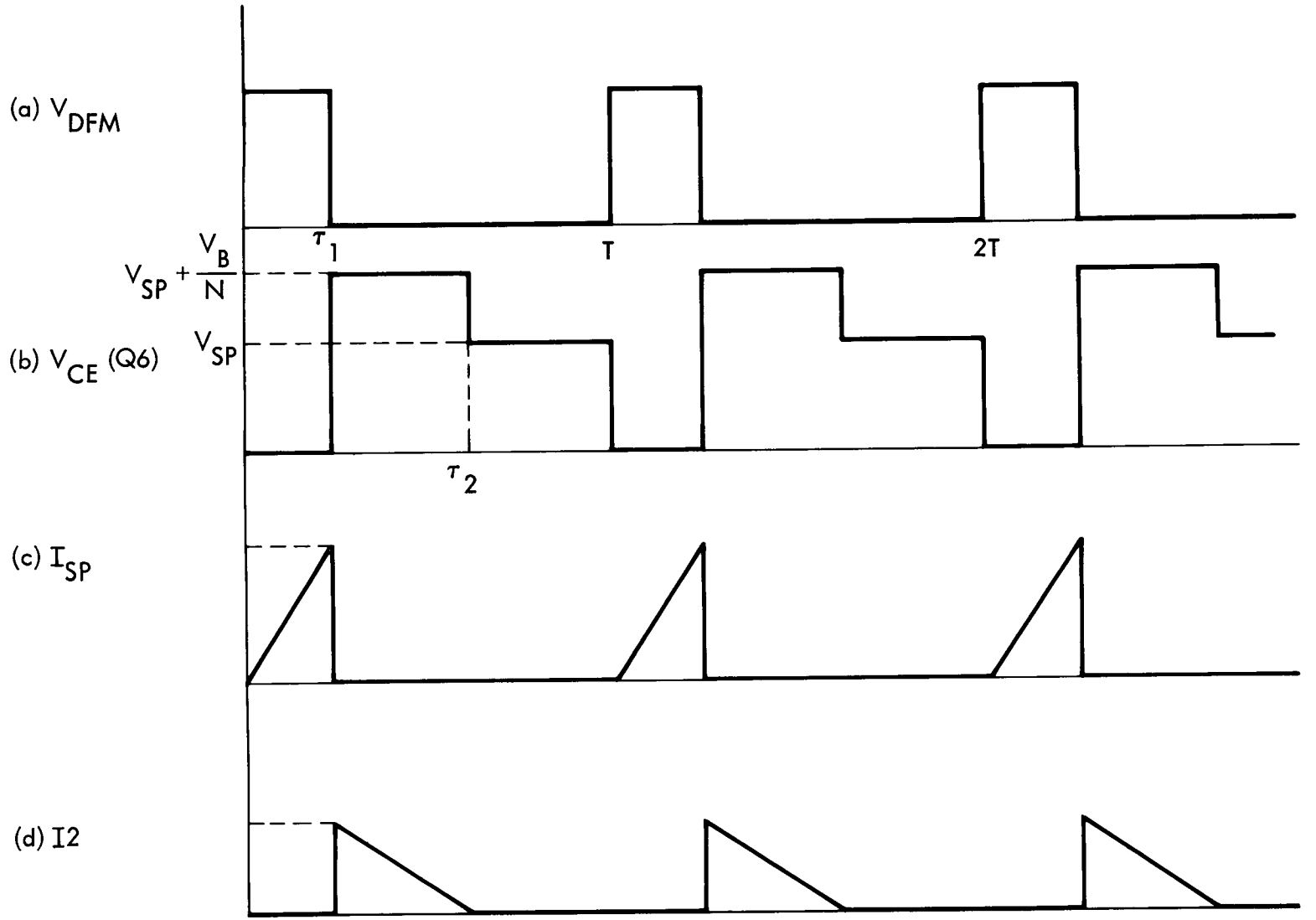


Figure 5.2-2. Switching circuit waveforms.

Under worst-case positive input conditions, it is desired to show that Q_6 is saturated. The following approach is used.

1. Prove that Q_1 saturates
2. Prove that Q_3 saturates
3. Prove that Q_7 is "off"
4. Determine R such that Q_6 saturates
5. Prove that Q_4 is in saturation

Q_1 is saturated under worst-case conditions if:*

$$\beta_{f_{1\,max}} \leq \beta_{1\,min} \tag{5.2-1}$$

Find $\beta_{f_{1\,max}}$.

$$\beta_{f_{1\,max}} = \frac{I_{c_{1\,max}}}{I_{b_{1\,min}}} \tag{5.2-2}$$

$$I_{c_{1\,max}} = I_{4\,max} + I_{3\,max} \tag{5.2-3}$$

$$I_{3\,max} = \frac{V_{2\,max} - V_{3\,max}}{R_{8\,min}} \tag{5.2-4}$$

$$**V_{2\,max} = E_{1\,max} - V_{be_{3\,min}} = 9.5 \text{ volts} \tag{5.2-5}$$

$$V_{3\,max} = E_{3\,max} + V_{ce_{1\,min}} = -5.0 \text{ volts} \tag{5.2-6}$$

Substituting $V_{2\,max}$ and $V_{3\,max}$ into Eq. (5.2-5) yields

$$I_{3\,max} = 0.385 \text{ ma.}$$

*Note maximum and minimum are defined as absolute quantities.

e.g. $E_3 = -5$ volts, $E_{3\,max} = -5.1$ volts, $E_{3\,min} = -4.9$ volts

**A table of critical parameters is provided in Table 5.2-1. Currents are defined according to Figure 5.2-1.

Symbol	Minimum	Maximum
E_1	9.9 volts	10.1 volts
E_2	4.9 volts	5.1 volts
E_3	-4.9 volts	-5.1 volts
RTN	0 volts	0 volts
R_5	4.0K	6.0K
R_6	0.8K	1.2K
R_7	4.0K	
R_8	37.6K	56.4K
R_9		12.0K
R_{10}	8K	
R_{17}	80K	
V_{CR_1}	0.6 volt	
V_{CR_2}		0.6 volt
I_{sp}	6 Amp. (50W)	13 Amp. (250W)
β_1	60	
V_{be_1}		0.8 volt
V_{ce_1}	0.1 volt	0.3 volt

Table 5.2-1. Table of critical parameters for block 2.

Symbol	Minimum	Maximum
β_2	35	
V_{be_2}		0.6 volt
V_{ce_2}		0.3 volt
β_3	15	
V_{be_3}	0.6 volt	0.8 volt
V_{ce_3}	0 volts	0.3 volt
β_4	70	
V_{be_4}	0.6 volt	0.7 volt
V_{ce_4}	0 volts	0.2 volt
β_5	30	
V_{be_5}	0.6 volt	0.9 volt
β_6	20	
V_{be_6}	1 volt	1.5 volts
β_7	35	
V_{be_7}	0.5 volt	1 volt
$^{+}V_{DFM}$	4.7 volts	

Table 5.2-1. (continued)

Assuming Q_2 is "off,"

$$I_{4\ max} = \frac{V_{10\ max}}{R_{6\ min}} \qquad (5.2\text{-}7)$$

$$V_{10\ max} = V_{3\ max} + V_{CR_{1\ min}} = -4.4 \text{ volts} \qquad (5.2\text{-}8)$$

Therefore,

$$I_{4\ max} = 5.5 \text{ ma.}$$

Substituting $I_{4\ max}$ and $I_{3\ max}$ into Eq. (5.2-3) yields

$$I_{c_{1\ max}} = 5.885 \text{ ma.}$$

$$I_{b_{1\ min}} = I_{1\ min} - I_{2\ max} \qquad (5.2\text{-}9)$$

$$I_{1\ min} = \frac{+V_{DFM} - V_{1\ min}}{R_{9\ max}} \qquad (5.2\text{-}10)$$

$$V_{1\ min} = E_{3\ min} + V_{be_{1\ max}} = -4.1 \text{ volts} \qquad (5.2\text{-}11)$$

$$I_{1\ min} = 0.735 \text{ ma}$$

$$I_{2\ max} = \frac{V_{be_{1\ max}}}{R_{10\ min}} = 0.1 \text{ ma}$$

Substituting $I_{1\ min}$ and $I_{2\ max}$ into Eq. (5.2-9) yields

$$I_{b_{1\ min}} = 0.635 \text{ ma.}$$

Substituting $I_{c_{1\ max}}$ and $I_{b_{1\ min}}$ into Eq. (5.2-2) yields

$$\beta_{f_1} = 9.25.$$

From equation (5.2-1),

$$\beta_{f_1} = 9.25 < 60 = \beta_{1\ min}.$$

Therefore, Q_1 is saturated.

Q_3 is saturated under worst-case conditions if:

$$\beta_{f_{3\ max}} \leq \beta_{3\ min.} \tag{5.2-12}$$

Find $\beta_{f_{3\ max}}$.

$$\beta_{f_{3\ max}} = \frac{I_{c_{3\ max}}}{I_{b_{3\ min}}} \tag{5.2-13}$$

$$I_{b_{3\ min}} = I_{3\ min} - I_{5\ max} \tag{5.2-14}$$

$$I_{5\ max} = \frac{V_{be_{3\ max}}}{R_{17\ min}} = 10\mu\ amp \tag{5.2-15}$$

$$I_{3\ min} = \frac{V_{2\ min} - V_{3\ max}}{R_{8\ max}} \tag{5.2-16}$$

$$V_{2\ min} = E_{1\ min} - V_{be_{3\ max}} = 9.1\ volts \tag{5.2-17}$$

$$V_{3\ max} = E_{3\ min} + V_{ce_{1\ max}} = -4.6\ volts \tag{5.2-18}$$

Substituting $V_{2\ min}$ and $V_{3\ max}$ into Eq. (5.2-16) yields

$$I_{3\ min} = 0.243\ ma.$$

Substituting $I_{3\ min}$ and $I_{5\ max}$ into Eq. (5.2-14) yields

$$I_{b_{3\ min}} \cong I_{3\ min} = 0.243\ ma. \tag{5.2-19}$$

$$I_{c_{3\ max}} = \frac{V_{5\ max} - V_{4\ min}}{R_{5\ min}} \tag{5.2-20}$$

$$V_{5\ max} = E_{1\ max} - V_{ce_{3\ min}} = 10.1\ volts \tag{5.2-21}$$

$$V_{4\ min} = V_{be_{6\ min}} + V_{be_{5\ min}} + V_{be_{4\ min}} = 2.2\ volts \tag{5.2-22}$$

Substituting $V_{5\ max}$ and $V_{4\ min}$ into Eq. (2-20) yields

$$I_{c_{3\ max}} = 1.98 \text{ ma.}$$

Substituting $I_{c_{3\ max}}$ and $I_{b_{3\ min}}$ into Eq. (5.2-13) yields

$$\beta_{f_{3\ max}} = 8.14.$$

From Eq. (5.2-12),

$$\beta_{f_{3\ max}} = 8.14 < 15 = \beta_{3\ min}.$$

Therefore, Q_3 is saturated under worst-case conditions.
Q_7 is "off" if:

$$V_{6\ max} < E_3 + V_{be_{7\ min}}.$$

Find $V_{6\ max}$.

$$V_{6\ max} = E_3 + V_{ce_{1\ max}} + V_{CR_{1\ min}} - V_{be_{2\ min}} = -4.7 \text{ volts} \quad (5.2\text{-}15)$$

$$V_{6\ max} = -4.7 \text{ volts} < -4.5 \text{ volts} = E_3 + V_{be_{7\ min}}$$

Therefore, Q_7 is "off" under worst-case conditions.
To determine R such that Q_6 will saturate,

$$\beta_{f_{6\ max}} = \frac{I_{sp\ max}}{I_{b_{6\ min}}}. \quad (5.2\text{-}16)$$

$$\text{Let } \beta_{6\ min} = \beta_{f_{6\ max}} = 20 \quad (5.2\text{-}17)$$

From Eq. (5.2-16),

$$I_{b_{6\ min}} = \frac{I_{sp\ max}}{\beta_{f_{6\ max}}} = 0.65 \text{ amp} \quad (5.2\text{-}18)$$

$$I_{b_{6\ min}} = I_{b_{4\ min}} + I_{7\ min} \tag{5.2-19}$$

$$I_{b_{4\ min}} = I_{c_{3\ min}} - I_{c_{2\ max}} \tag{5.2-20}$$

Since Q_7 is "off",

$$I_{c_{2\ max}} = I_{9\ max} \tag{5.2-21}$$

$$I_{9\ max} = \frac{V_{10\ max} - V_{be_{2\ min}} - E_3}{R_{7\ min}} \tag{5.2-22}$$

$V_{10\ max}$ is found in Eq. (5.2-8)

$$I_{9\ max} = 0\ ma$$

i.e.: Q_2 is "off".

From Eq. (5.2-20),

$$I_{b_{4\ min}} = I_{c_{3\ min}}. \tag{5.2-23}$$

$$I_{c_{3\ min}} = \frac{V_{5\ min} - V_{4\ max}}{R_{5\ max}} \tag{5.2-24}$$

$$V_{5\ min} = E_{1\ min} - V_{ce_{3\ max}} = 9.6\ volts \tag{5.2-25}$$

$$V_{4\ max} = V_{be_{6\ max}} + V_{be_{5\ max}} + V_{be_{4\ max}} = 3.1\ volts \tag{5.2-26}$$

Substituting $V_{5\ min}$ and $V_{4\ max}$ into Eq. (5.2-24) yields

$$I_{c_{3\ min}} = 1.08\ ma = I_{b_{4\ min}}.$$

From Eq. (5.2-19),

$$I_{7\ min} = I_{b_{6\ min}} - I_{b_{4\ min}} \cong 0.65\ amp \tag{5.2-27}$$

I_7 minimum must be delivered under worst-case conditions (i.e., minimum supply and maximum V_9).

$$R_{max} = \frac{E_{2\ min} - V_{9\ max}}{I_{7\ min}} \qquad (5.2\text{-}28)$$

Let R_{max} be a 1 percent resistor with 5 percent overall tolerance.

$$R_{max} = \frac{E_{2\ min} - V_{9\ max}}{1.05\ I_{7\ min}} \qquad (5.2\text{-}29)$$

$$V_{9\ max} = V_{be_{6\ max}} + V_{be_{5\ max}} + V_{ce_{4\ max}} = 2.6 \text{ volts} \qquad (5.2\text{-}30)$$

$$R_{max} = 3.35\ \Omega,\ 1\%,\ 5 \text{ watt}$$

The above R_{max} is a recommended change from R = 3.9 Ω, ±5 percent, 3 watt resistor in the 250 watt OCR

Q_4 is saturated if:

$$\beta_{f_{4\ max}} \leq \beta_{4\ min} \qquad (5.2\text{-}31)$$

$$\beta_{f_{4\ max}} = \frac{I_{c_{4\ max}}}{I_{b_{4\ min}}} \qquad (5.2\text{-}32)$$

$$I_{c_{4\ max}} \cong \frac{I_{c_{5\ max}}}{\beta_{5\ min}} \approx \frac{I_{7\ max}}{\beta_{5\ min}} \qquad (5.2\text{-}33)$$

$$I_{7\ max} = \frac{E_{2\ max} - V_{9\ min}}{R_{min}} \qquad (5.2\text{-}34)$$

$$V_{9\ min} = V_{be_{6\ min}} + V_{be_{5\ min}} + V_{ce_{4\ min}} = 1.6 \text{ volts} \qquad (5.2\text{-}35)$$

$$R_{min} = 3.19\ \Omega$$

$$I_{7\ max} = 1.1 \text{ amp}$$

Substituting into Eq. (5.2-33) yields

$$I_{c_{4\ max}} = 36.6\ ma.$$

Substituting $I_{b_{6\ min}}$ (Eq. 5.2-18) and $I_{c_{4\ max}}$ into Eq. (5.2-32) yields

$$\beta_{f_{4\ max}} = 38.$$

From Eq. (5.2-31),

$$\beta_{f_{4\ max}} = 38 < 70 = \beta_{4\ min}. \qquad (5.2\text{-}36)$$

Therefore, Q_4 is saturated under worst-case conditions.

Now the "on" case for the 50 watt regulator will be considered.

There are three components in the 50 watt regulator which are different from the 250 watt regulator. These are: R_6, R_3 and R. Analysis will proceed to determine if these changes affect worst-case operation.

R_6 affects the "on" condition of Q_1. Q_1 is in saturation if:

$$\beta_{f_{1\ max}} \leq \beta_{1\ min} \qquad (5.2\text{-}1)$$

$$\beta_{f_{1\ max}} = \frac{I_{c_{1\ max}}}{I_{b_{1\ min}}} \qquad (5.2\text{-}2)$$

$I_{b_{1\ min}}$ is the same as the 250 watt case.

$$I_{b_{1\ min}} = 0.635\ ma$$

$$I_{c_{1\ max}} = I_{4\ max} + I_{3\ max} \qquad (5.2\text{-}3)$$

$I_{3\ max}$ is identical in both cases.

$$I_{3\ max} = 0.385\ ma$$

$$I_{4\ max} = \frac{V_{10\ max}}{R_{6\ min}} = 1.83\ ma \qquad (5.2\text{-}7)$$

Substituting into Eq. (5.2-3) yields

$$I_{c_{1\ max}} = 2.215\ ma.$$

Substituting into Eq. (5.2-2) yields

$$\beta_{f_{1\ max}} = 3.5.$$

From Eq. (5.2-1),

$$\beta_{f_{1\ max}} = 3.5 < 60 = \beta_{1\ min}.$$

Therefore, Q_1 is saturated under worst-case conditions.

Component R_3 has little effect on the circuit operation. To determine the maximum value of R,

$$R_{max} = \frac{E_{2\ min} - V_{9\ max}}{1.05\ I_{7\ min}}. \qquad (5.2\text{-}29)$$

$V_{9\ max}$ remains unchanged.

$$V_9 = 2.6\ volts \qquad (5.2\text{-}30)$$

$$I_{7\ min} = I_{b_{6\ min}} - I_{b_{4\ min}} \qquad (5.2\text{-}27)$$

Assuming $I_{b_{4\ min}} \ll I_{b_{6\ min}}$,

$$I_{7\ min} \approx I_{b_{6\ min}} \tag{5.2-37}$$

$$I_{b_{6\ min}} = \frac{I_{sp\ max}}{\beta_{f_{6\ max}}} = 0.3\ amp \tag{5.2-18}$$

Substituting into Eq. (5.2-29) yields

$$R_{max} = 7.15\Omega,\ 1\%,\ 3\ watt.$$

The above R_{max} is a recommended change from R = 15Ω, ±5 percent 1/2 watt in the 50 watt regulator.

Under worst-case negative DFM input conditions, it is desired to show that Q_6 is "off". The following approach is taken:

1. prove that Q_1 is "off"
2. prove that Q_2 is saturated
3. prove that Q_6 is "off"

It can be seen from Figure 5.2-3, that when the power amplifier transistor turns "off," the base of Q_1 is open circuited. Therefore, Q_1 is "off" under worst-case conditions.

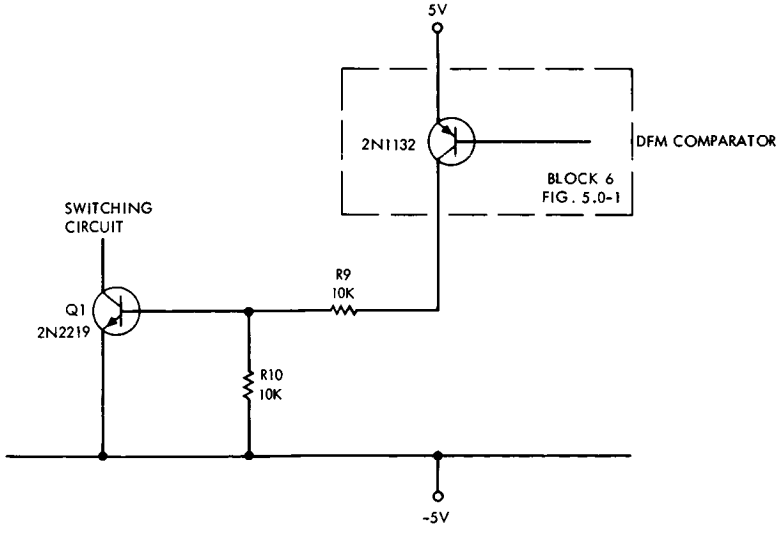


Figure 5.2-3. Driving circuit.

As Q_1 turns "off," I_3 approaches zero. Q_3 begins to turn "off" which back biases CR_1 and forward biases CR_2. Assuming Q_2 goes into saturation, Q_6 should turn "off".

Q_2 is saturated if:

$$\beta_{f_{2\ max}} \leq \beta_{2\ min} \tag{5.2-38}$$

$$\beta_{f_{2\ max}} = \frac{I_{c_{2\ max}}}{I_{b_{2\ min}}} \tag{5.2-39}$$

$$I_{b_{2\ min}} = \frac{V_{10\ min}}{R_{6\ max}} \tag{5.2-40}$$

$$V_{10\ min} = E_{3\ min} - V_{be_{7\ max}} - V_{be_{2\ max}} = -3.3 \text{ volts} \tag{5.2-41}$$

$$I_{b_{2\ min}} = 2.75 \text{ ma}$$

$$I_{c_{2\ max}} = I_{b_{7\ max}} + I_{9\ max} - I_{b_{2\ min}} \tag{5.2-42}$$

$$I_{b_{7\ max}} \approx \frac{I_{7\ max}}{\beta_{7\ min}} = 31.5 \text{ ma} \tag{5.2-43}$$

$$I_{9\ max} = \frac{V_{be_{7\ max}}}{R_{7\ min}} = 0.25 \text{ ma} \tag{5.2-44}$$

Substituting into Eq. (5.2-42) yields

$$I_{c_{2\ max}} = 29.2 \text{ ma.}$$

From Eq. (5.2-39),

$$\beta_{f_{2\ max}} = 10.6.$$

From Eq. (5.2-38),

$$\beta_{f_{2\ max}} = 10.6 < 35 = \beta_{2\ min}.$$

Therefore, Q_2 is saturated under worst-case conditions.
Q_6 is "off" if:

$$V_{b_{6\ max}} \leq RTN + V_{be_{6\ min}} = 1.0 \text{ volts} \qquad (5.2\text{-}45)$$

$$V_{b_{6\ max}} = V_{6\ max} + V_{ce_{2\ max}} + V_{CR_{2\ max}} \qquad (5.2\text{-}46)$$

$$V_{6\ max} = E_{3\ min} + V_{be_{7\ max}} = -3.9 \text{ volts} \qquad (5.2\text{-}47)$$

$$V_{b_{6\ max}} = -3.0 \text{ volts}$$

From Eq. (5.2-45),

$$V_{b_{6\ max}} = -3.0 \text{ volts} < RTN + V_{be_{6\ min}} = 1.0 \text{ volts}$$

Therefore, Q_6 is "off" under worst-case conditions. All components are the same in the 250 watt and 50 watt regulators for the "off" case analysis; therefore, Q_6 in the 50 watt regulator will also turn "off" under worst-case conditions.

5.2.2 Stress Analysis

A stress analysis was performed on the switching circuit to insure that none of the components are over stressed. It was found that CR_2 is required to deliver very nearly its rated current. This problem can be resolved by replacing the 1N3730 (CR_2) with a 1N4245 diode. Table 5.2-2 is a summary of the stress analysis for block 2.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation (mw)*			Power Dissipation (mw)*		
Transistors			Vceo (volts)			Vceo (volts)	
Q_1	2N2219	800	40		< 1	15	
Q_2	2N2219	800	40		< 1	10	
Q_3	2N1132	1 watt	35		< 1	10	
Q_4	2N2219	800	40		2	5	
Q_5	2N2893	17 watts	80		358	5	
Q_6	2N3599	100 watts	80		1.65 watts	50	
Q_7	2N2893	17 watts	80		< 1	15	
Resistors							
R [250w]	3.35Ω	5 watts			0.2 watts		
R [50w]	7.15Ω	3 watts			0.9 watts		
R_3[250w]	1.0 Ω	250			< 1		
R_3[50w]	3.0 Ω	250			< 1		
R_5	5.1K	250			6		
R_6[250w]	1.0K	250			8		
R_6[50w]	3.0K	250			10		
R_7	5.1K	250			< 1		
R_8	47K	250			2		
R_9	10K	250			5		
R_{10}	10K	250			< 1		
R_{17}	100K	250			< 1		
			PIV	I_f		PIV	I_f
Diodes			volts	ma		volts	ma
CR_1	1N3600	500	50	200	2.5	15	6
CR_2	1N3730	750	60	1,500	70	10	1,100
Capacitors			(volts)			(volts)	
C_2	12μf		100			50	
C_1	.01μf		100			60	

*Unless otherwise noted.

Table 5.2-2. Stress analysis summary for block 2.

5.2.3 Conclusions

The switching circuit will work under worst-case conditions with the following alterations:

1. Change CR_2 (1N3730) to a higher current device such as the 1N4245.
2. For the 250 watt regulator, let R = 3.32Ω ±1 percent, 5 watts.
3. For the 50 watt regulator, let R = 7.15Ω ±1 percent, 3 watts.

5.3 DUTY FACTOR MODULATOR

The Duty Factor Modulator (DFM) adjusts the duty factor of the switching circuit such that the regulator operates about the solar panel maximum power point. The DFM consists of functional blocks 3 through 6, Figure 5.0-1.

Block 3, the astable oscillator, is a npn configuration in the 250 watt regulator, Figures 5.3-1 and 5.3-3. The 50 watt regulator uses pnp transistors in block 3, Figures 5.3-2 and 5.3-4.

Block 4 (Figure 5.4-1) is only necessary for the 4-phase 250 watt regulator. In the 50 watt 2-phase regulator block 3 is fed directly to block 5 as shown in Figure 5.3-2. Corresponding blocks 5 and 6 are the same in both regulators.

Figures 5.3-1 and 5.3-2 show only one phase of the 4-phase and 2-phase DFM respectively. This was done to simplify analysis, since all the phases for each regulator are the same.

5.3.1 Block 3, Astable Oscillator (250-W OCR)

In the 250 watt OCR, the 20-kHz astable oscillator block (Figure 5.3-3) generates the clock rate for the circuit.

The criteria for operation are:

1. The astable will oscillate under worst-case conditions.
2. The frequency will not vary more than ±10 percent.

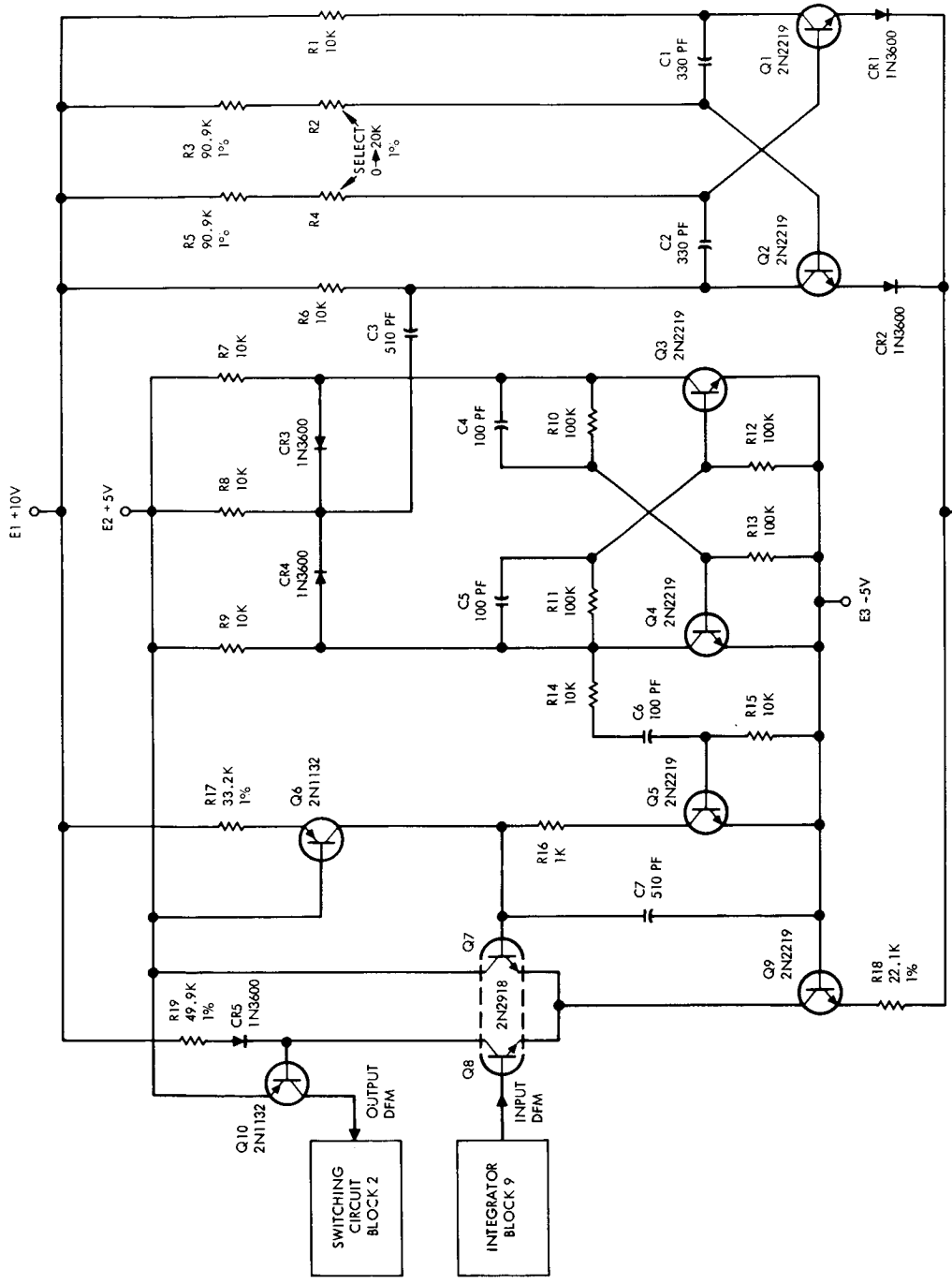


Figure 5.3-1. 250-W duty factor modulator (1 phase).

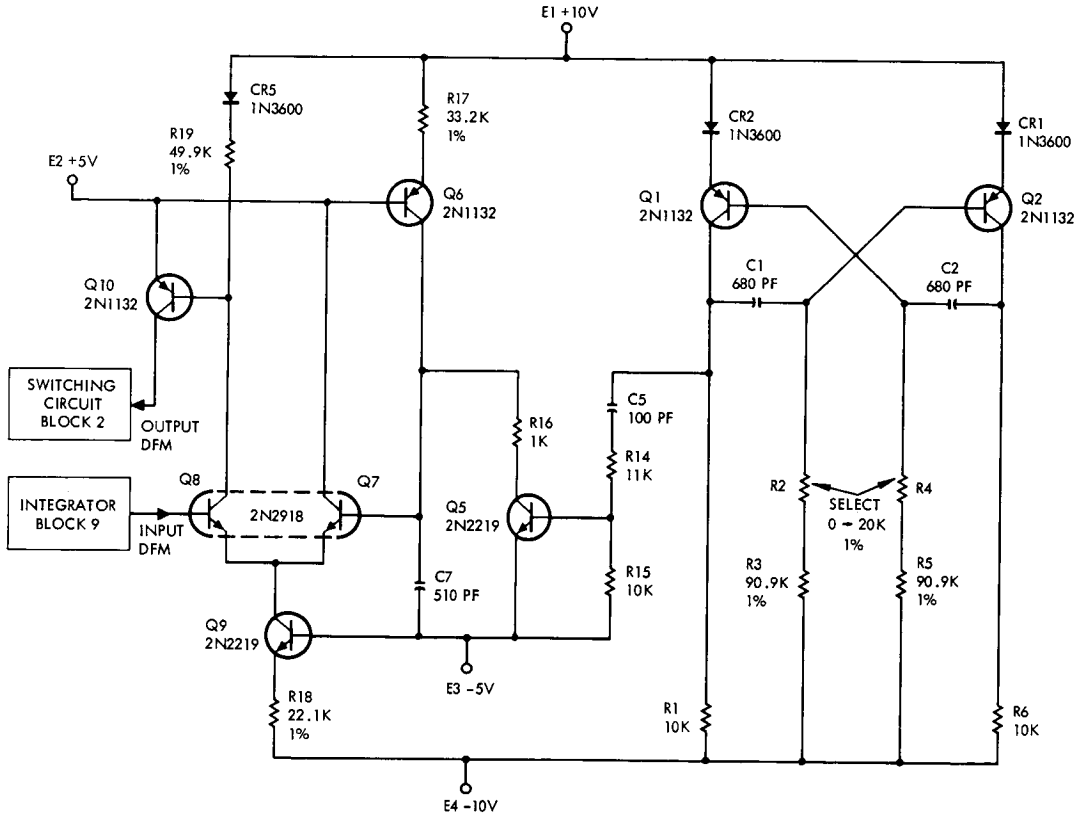


Figure 5. 3-2. 50-W duty factor modulator (1 phase).

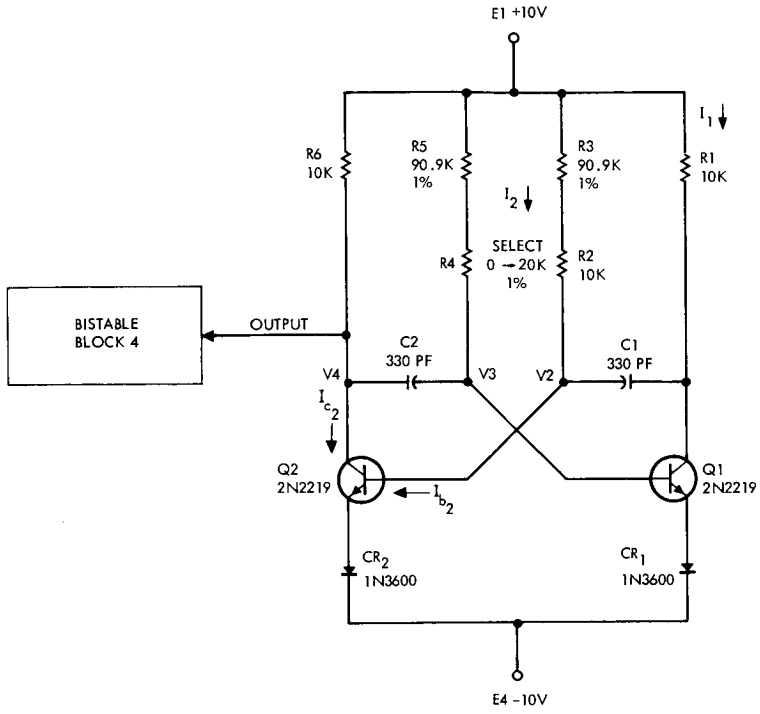


Figure 5.3-3. Astable oscillator block 3 (250-W OCR).

The oscillator will operate under worst case if Q_1 and Q_2 can cycle from full "on" to full "off." Assuming Q_1 is just "off" and Q_2 is "on" prove:

1. Q_2 is "on"
2. Q_1 is "off"

Considering the 250 watt OCR oscillator,

Q_2 is "on" if:

$$\beta_{f_{2\,max}} \leq \beta^{*}_{2\,min} \tag{5.3-1}$$

$$\beta_{f_{2\,max}} = \frac{I_{c_{2\,max}}}{I_{b_{2\,min}}} \tag{5.3-2}$$

*A table of critical parameters is provided in Table 5.3-1. Symbols are defined in Figure 5.3-3.

Symbol	Minimum	Maximum
E_1	9.9 volts	10.1 volts
E_4	-9.9 volts	-10.1 volts
R_2		10.5K
R_3		105K
R_6	8K	
V_{CR_1}	0.6 volt	0.6 volt
V_{CR_2}	0.6 volt	0.6 volt
250 watt parameters		
β_2	50	
V_{ce_2}	0 volt	0.6 volt
V_{be_1}	0.6 volt	0.6 volt
C_2		347 pf
50 watt parameters		
β_2	30	
V_{ce_2}		-1.5 volts
V_{be_1}	0	-1
C_2		715 pf

Table 5.3-1. Table of critical parameters for block 3.

$$I_{c_{2\,max}} = \frac{E_{1\,max} - V_{4\,min}}{R_{6\,min}} \qquad (5.3\text{-}3)$$

$$V_{4\,min} = V_{ce_{2\,min}} + V_{CR_{2\,min}} + E_{4\,max} = -9.5 \text{ volts} \qquad (5.3\text{-}4)$$

Substituting into Eq. (5.3-3) yields

$$I_{c_{2\,max}} = 2.45 \text{ ma.}$$

Assuming Q_1 is "off:"

$$I_{b_{2\ min}} = I_{1\ min} + I_{2\ min} \tag{5.3-5}$$

$$I_{2\ min} = \frac{E_{1\ min} - V_{2\ max}}{R_{2\ max} + R_{3\ max}} \tag{5.3-6}$$

$$V_{2\ max} = E_{4\ min} + V_{CR_{2\ max}} + V_{ce_{2\ max}} = -8.7 \text{ volts} \tag{5.3-7}$$

Substituting into Eq. (5.3-6) yields

$$I_{2\ min} = 0.162 \text{ ma.}$$

Assume:

$$I_{1\ min} = 0 \text{ ma.}$$

Substituting into Eq. (5.3-5) yields

$$I_{b_{2\ min}} = 0.162 \text{ ma.}$$

From Eq. (5.3-2),

$$\beta_{f_{2\ max}} = 15.$$

Comparing $\beta_{f_{2\ max}}$ with Eq. (5.3-1),

$$\beta_{f_{2\ max}} = 15 < 50 = \beta_{2\ min}.$$

Therefore, Q_2 will cycle "on" under worst-case conditions. Q_1 is "off" if:

$$V_{3\ min} < E_{4\ min} + V_{CR_{1\ max}} + V_{be_{1\ max}} = -8.7 \text{ volts} \tag{5.3-8}$$

$V_{3\ min}$ occurs just as Q_2 turns "on".

$$V_{3\ min} = V_3\ (Q_1\ \text{"on"}) + V_4\ (Q_2\ \text{"on"}) \qquad (5.3\text{-}9)$$

$$V_3(Q_1\ \text{"on"}) = E_4 + V_{CR_1} + V_{be_1} = -8.7\ \text{volts} \qquad (5.3\text{-}10)$$

$$V_4\ (Q_2\ \text{"on"}) = -9.5\ \text{volts} \qquad (5.3\text{-}4)$$

Therefore,

$$V_{3\ min} = -18.2\ \text{volts}.$$

From Eq. (5.3-8),

$$-18.2\ \text{volts} < -8.7\ \text{volts}.$$

Therefore, under worst-case conditions Q_1 will cycle "off." The frequency of operation is:

$$f = \frac{1}{1.38\ RC} \qquad (5.3\text{-}11)$$

where R is the base resistance, and C is the value of the speed up capacitor.

$$f_{min} = \frac{1}{1.38\ (R_5 + R_4)_{max}\ (C_2)_{max}} = 18.1\ \text{kHz} \qquad (5.3\text{-}12)$$

$$f_{max} = \frac{1}{1.38\ (R_5 + R_4)_{min}\ C_{2\ min}} = 21.9\ \text{kHz} \qquad (5.3\text{-}13)$$

5.3.2 Conclusion

Since this frequency range falls within the ±10% specification, the oscillator will work under worst-case conditions.

5.3.3 Block 3, Astable Oscillator (50-W OCR)

The 50 watt OCR astable oscillator (Figure 5.3-4) will now be considered. All biasing components are essentially the same for the oscillators in both regulators. Therefore the forcing betas are the same. Different transistors are used, however the basic analysis remains the same.

Q_2 is "on" if:

$$\beta_{f_{2\ max}} \leq \beta_{2\ min} \qquad (5.3\text{-}1)$$

$$\beta_{f_{2\ max}} = 15 < 30 = \beta_{2\ min}$$

Therefore, Q_2 will cycle "on" under worst-case conditions.

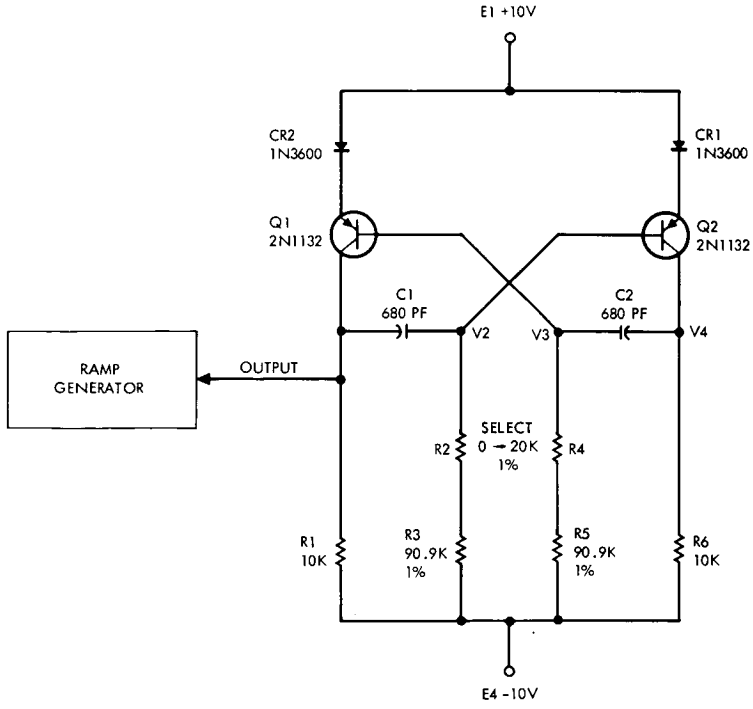


Figure 5.3-4. Astable oscillator block 3 (50-W OCR).

Q_1 is "off" if:

$$V_{3\ max} > E_{1\ max} - V_{CR_{2\ min}} - V_{be_{1\ min}} = +9.5 \text{ volts} \quad (5.3\text{-}14)$$

$$V_{3\ max} = V_3(Q_{1\ "on"}) + V_4(Q_{2\ "on"}) \quad (5.3\text{-}9)$$

$$V_3(Q_{1\ "on"}) = E_{1\ min} + V_{CR_{2\ max}} + V_{be_{1\ max}} = +8.3 \text{ volts} \quad (5.3\text{-}15)$$

$$V_4(Q_{2\ "on"}) = E_{1\ min} - V_{CR_{1\ max}} + V_{ce_{2\ max}} = 7.8 \text{ volts} \quad (5.3\text{-}16)$$

Therefore,

$$V_{3\ max} = 16.1 \text{ volts.}$$

From Eq. (5.3-14),

$$16.1 \text{ volts} > 9.5 \text{ volts.}$$

Therefore, Q_1 will cycle "off" under worst-case conditions.
The frequency range is as follows:

$$f_{min} = \frac{1}{1.38\,(R_5 + R_4)_{max}\,(C_2)_{max}} = 9 \text{ kHz} \quad (5.3\text{-}12)$$

$$f_{max} = \frac{1}{1.38\,(R_5 + R_4)_{min}\,(C_2)_{min}} = 11 \text{ kHz} \quad (5.3\text{-}13)$$

5.3.4 Conclusion

Since this frequency range falls within the ±10% specification, the oscillator will work under worst-case conditions.

5.3.5 Stress Analysis

A stress analysis was performed on the oscillators to insure that components were not over stressed. A summary of results is found in Table 5.3-2.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation (mw)*			Power Dissipation (mw)*		
Transistors			Vceo (volts)			Vceo (volts)	
Q_1 and Q_2 [250w]	2N2219	800	40		<1	20	
Q_1 and Q_2 [50w]	2N1132	1 watt	35		<1	20	
Resistors							
R_1	10K	250			37		
R_2	0→20K select	125			<1		
R_3	90.9K	125			4		
R_4	0→20K select	125			<1		
R_5	90.9K	125			4		
R_6	10K	250			37		
			PIV	I_f		PIV	I_f
Diodes			volts	ma		volts	ma
CR_1 and CR_2	1N3600	500	50	200	1	20	2
Capacitors			(volts)			(volts)	
C_1 and C_2 [250w]	330pf		500			20	
C_1 and C_2 [50w]	680pf		500			20	

*Unless otherwise noted.

Table 5.3-2. Stress analysis summary for block 3.

5.4 BLOCK 4, BISTABLE FLIP-FLOPS

The 20 kHz oscillator output is fed into two bistable flip-flops which in turn generate clock pulses to control four ramp generators. A functional block diagram is shown in Figure 5.4-1.

Figure 5.4-2 is a schematic diagram of block 4. Components R_7, R_8, R_9, CR_4, CR_3 and C_3 comprise the pulse generating circuit which commands the flip-flop.

The criteria for operation are as follows:

1. When Q_3 is "on", Q_4 is to be "off" and vice versa.
2. The triggering time constant, τ_{C_3} is to be smaller than the flip-flop's time constant, τ_{C_5}.
3. The bistable frequency response is to be greater than the command pulse frequency.

Q_3 is "on" if:

$$\beta_{f_{3\ max}} \leq \beta_3^{*}{}_{min}. \tag{5.4-1}$$

Assuming Q_4 is "off."

$$\beta_{f_{3\ max}} = \frac{I_{c_{3\ max}}}{I_{b_{3\ min}}} \tag{5.4-2}$$

$$I_{c_{3\ max}} = \frac{E_{2\ max} - V_{7\ min}}{R_{7\ min}} \tag{5.4-3}$$

$$V_{7\ min} = E_{3\ max} + V_{ce_{3\ min}} = -5.1 \text{ volts} \tag{5.4-4}$$

*A table of critical parameters is found in Table 5.4-1.

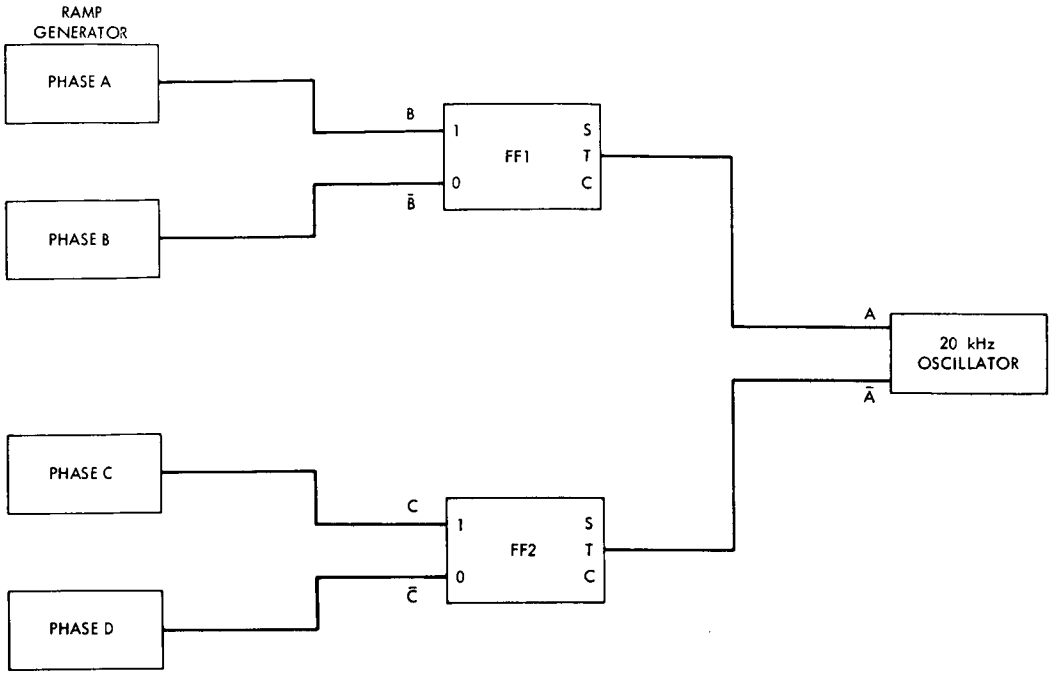


Figure 5.4-1. Functional block diagram, block 4.

Therefore,

$$I_{c_{3\ max}} = 1.28\ ma.$$

$$I_{b_{3\ min}} = \frac{E_{2\ max} + V_{6\ max}}{(R_9 + R_{11})_{max}} \qquad (5.4\text{-}5)$$

$$V_{6\ max} = E_{3\ max} + V_{be_{3\ min}} = -4.5\ volts \qquad (5.4\text{-}6)$$

Substituting into Eq. (5.4-5),

$$I_{b_{3\ min}} = 7.3 \times 10^{-5}\ amp.$$

From Eq. (5.4-2),

$$\beta_{f_{3\ max}} = 17.6.$$

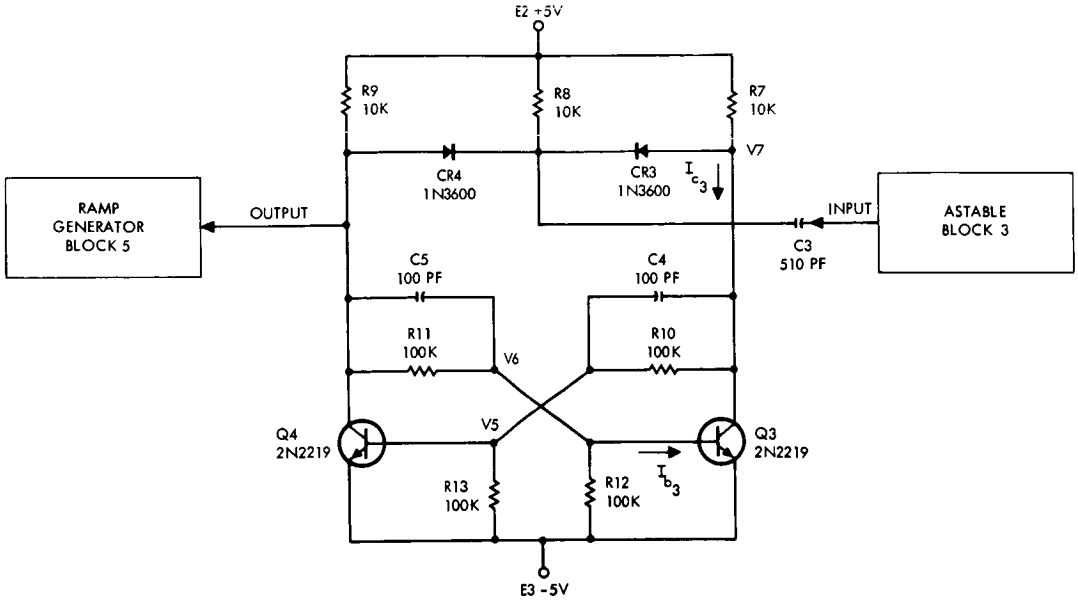


Figure 5.4-2. Bistable multivibrator flip flop

From Eq. (5.4-1),

$$\beta_{f_{3\ max}} = 17.6 < 50 = \beta_{3\ min}.$$

Therefore, Q_3 is "on" under worst-case conditions.
Q_4 is "off" if:

$$V_5\ (Q_{4\ \text{"off"}})_{max} < V_5\ (Q_{4\ \text{"on"}})_{min} \qquad (5.4\text{-}7)$$

$$V_5\ (Q_{4\ \text{"off"}})_{max} = E_{3\ max} + V_{ce_{3\ max}} = -4.8 \text{ volts} \qquad (5.4\text{-}8)$$

$$V_5\ (Q_{4\ \text{"on"}})_{min} = E_{3\ max} + V_{be_{4\ min}} = -4.5 \text{ volts} \qquad (5.4\text{-}9)$$

Substituting into Eq. (5.4-7),

$$-4.8 \text{ volts} < -4.5 \text{ volts}.$$

Therefore Q_4 is "off" under worst-case conditions. It can be seen that due to symmetry, Q_4 will be "on" when Q_3 is "off".

The triggering pulse must have a shorter rise time (τ_{C_3}) than the rise time of the flip-flop (τ_{C_5}) to insure triggering. Figure 5.4-3 is the equivalent circuit model used to find the trigger rise time, τ_{C_3}.

Under worst-case conditions,

$$\tau_{C_{3\ max}} < \tau_{C_{5\ min}} \tag{5.4-10}$$

$$\tau_{C_{3\ max}} = R_{max}\, C_{3\ max} \tag{5.4-11}$$

$$R_{max} = R_{9\ max} // R_{8\ max} // R_{7\ max} = 4K \tag{5.4-12}$$

Therefore,

$$\tau_{C_{3\ max}} = 2.14\ \mu sec.$$

Figure 5.4-4 is the equivalent circuit used to find the rise time of the flip-flop.

$$\tau_{C_{5\ min}} = R_{min}\, C_{5\ min} \tag{5.4-13}$$

$$R_{min} = \frac{R_{11\ min}\, R_{12\ min}}{R_{11\ min} + R_{12\ min}} = 40K \tag{5.4-14}$$

Therefore,

$$\tau_{C_{5\ min}} = 3.8\ \mu sec.$$

From Eq. (5.4-10),

$$\tau_{C_{3\ max}} = 2.14\ \mu sec < 3.8\ \mu sec = \tau_{C_{5\ min}}.$$

Since the time constants are nearly the same, it is suggested that C_4 and C_5 be changed from 100 pf to 300 pf.

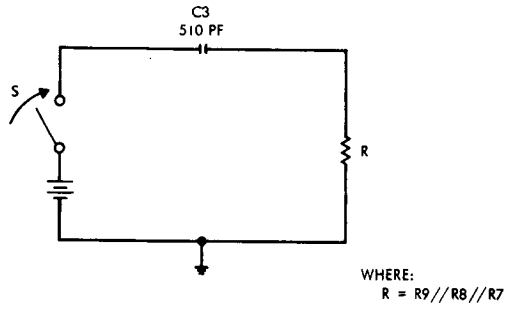


Figure 5.4-3. Equivalent pulse circuit.

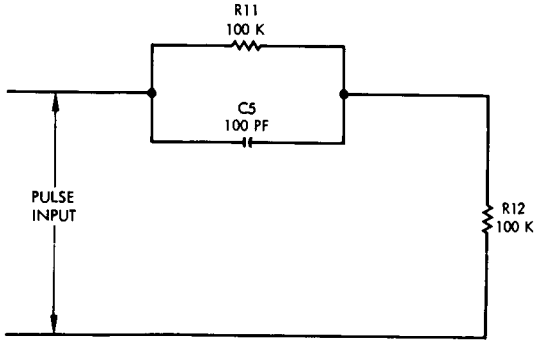


Figure 5.4-4. Flip flop rise time equivalent circuit.

Symbol	Minimum	Maximum
E_2		5.1 volts
E_3		-5.1 volts
R_7	8K	12K
R_8		12K
R_9		12K
R_{11}	80K	120K
R_{12}	80K	120K
β_3	50	
V_{ce_3}	0 volt	0.3 volt
V_{be_3}	0.6 volt	
V_{be_4}	0.6 volt	
C_3		535.5 pf
C_5*	95 pf	
C_5**	285 pf	315 pf
*Original Design		
**Suggested change		

Table 5.4-1. Table of critical parameters for block 4.

Substituting the new value of capacitance into Eq. (5.4-13),

$$\tau_{C_{5\ min}} = 11.4\ \mu sec.$$

From Eq. (5.4-10),

$$\tau_{C_{3\ max}} = 2.14\ \mu sec << 11.4\ \mu sec = \tau_{C_{5\ min}}.$$

If the above change is incorporated, a triggering pulse is insured under worst-case conditions.

To guarantee switching when a command triggering pulse is delivered, the operating frequency should be less than one-half of the flip-flop's natural frequency. The natural frequency is:

$$f_n = \frac{R_{11} + R_{12}}{R_{11} R_{12} C_5} \qquad (5.4\text{-}15)$$

The flip-flop will work if:

$$f_{max} < \frac{f_{n\,min}}{2} \qquad (5.4\text{-}16)$$

$$\frac{f_{n\,min}}{2} = \frac{R_{11\,max} + R_{12\,max}}{2R_{11\,max} R_{12\,max} C_{5\,max}} = 26.5 \text{ kHz} \qquad (5.4\text{-}17)$$

The maximum operating frequency is found from block 3 Eq. (5.3-13).

$$f_{max} = 21.9 \text{ kHz}$$

From Eq. (5.4-16),

$$f_{max} = 21.9 \text{ kHz} < 26.5 \text{ kHz} = \frac{f_{n\,min}}{2}$$

5.4.1 Conclusion

If C_4 and C_5 are changed to 300 pf, all of the criteria for reliable operation can be met and the flip-flop will operate under worst-case conditions.

5.4.2 Stress Analysis

A stress analysis was performed on block 4 and the results can be found in Table 5.4-2.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation (mw)*			Power Dissipation (mw)*		
Transistors			Vceo (volts)			Vceo (volts)	
Q_3 and Q_4	2N2219	800	40		<1	10	
Resistors							
R_7	10K	250			2		
R_8	10K	250			<1		
R_9	10K	250			2		
R_{10}	100K	250			<1		
R_{11}	100K	250			<1		
R_{12}	100K	250			<1		
R_{13}	100K	250			<1		
			PIV	I_f		PIV	I_f
Diodes			(volts)	(ma)		(volts)	(ma)
CR_1 and CR_2	1N3600	500	50	200		15	2
Capacitors			(volts)			(volts)	
C_3	510pf		500			15	
C_4 and C_5	300pf		500			10	

*Unless otherwise noted.

Table 5.4-2. Stress analysis summary for block 4.

5.5 BLOCK 5, RAMP GENERATOR

The ramp generator, Figure 5.5-1, develops a voltage which is proportional to time and is synchronized by the astable oscillator. The comparator compares the ramp generator output with the integrator output. At their zero crossover point, the comparator output changes states.

The ramp generator operates in the following manner. Assume C_7 (Figure 5.5-1) is completely discharged. At t = 0 (Figure 5.5-2) C_7 charges at a constant rate by means of the current generator, Q_6, until the voltage across C_7 approaches E_2 at $t = t_1$. At this time Q_6 saturates and there is no further increase in the voltage across C_7. A pulse at the input of Q_5 at $t = t_2$ turns "on" Q_5 and discharges C_7 quickly. At the termination of the pulse Q_5 turns "off" ($t = t_3$) and C_7 begins to charge again.

The following criteria are necessary for circuit operation.

1. C_7 must completely discharge before Q_5 turns "off".
2. C_7 must completely charge before Q_5 turns "on".
3. The comparator outputs must not differ by more than ten percent per period.

5.5.1 Worst Case Analysis, Ramp Generator (250-W OCR)

The 250 watt regulator will be considered first. It is necessary for Q_5 to remain "on" for a period of time sufficient to discharge C_7 under worst case conditions. Referring to Figure 5.5-1, it can be seen that the maximum discharge time, τ_{7max}, required is:

$$*\tau_{7max} = 4\,(R_{16max}\,C_{7max}) = 2.58\,\mu sec. \qquad (5.5\text{-}1)$$

It is assumed that four time constants are required to discharge C_7.

*A table of critical parameters is found in Table 5.5-1.

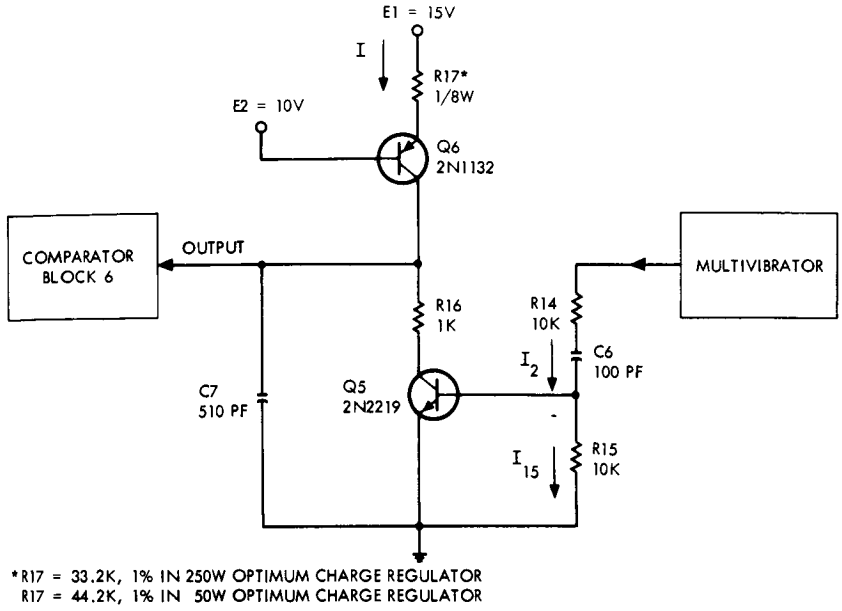


Figure 5.5-1. Block 5 ramp generator.

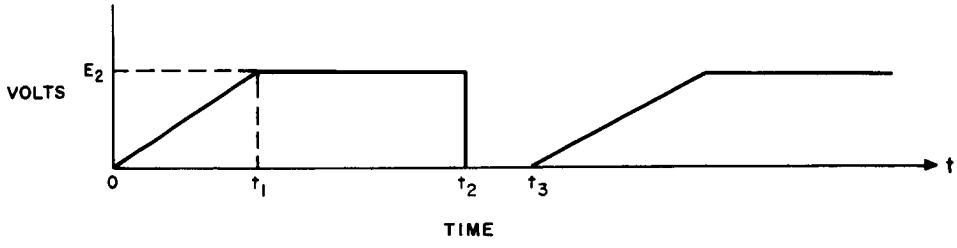


Figure 5.5-2. Ramp generator output.

Symbol	Minimum	Maximum
E_1	14. 8 volts	15. 2 volts
E_2	9. 8 volts	10. 2 volts
R_7	8K	12K
R_{11}	80K	120K
R_{14}	8K	12K
R_{15}	8K	12K
R_{16}	0. 8K	1. 2K
R_{17}	31. 5K	34. 88K
C_5	285 pf	315 pf
C_6	95 pf	105 pf
C_7	485 pf	535 pf
V_{be_5}	0. 6 volt	0. 6 volt
V_{be_6}	0. 6 volt	0. 6 volt
V_{in}	8. 8 volts	9. 2 volts

Table 5. 5-1. Table of critical parameters (250-W OCR) for block 5. .

Q_5 will turn "on" when a positive pulse is applied to its base. The length of the pulse determines the "on" time of Q_5, and therefore, must be considered. This pulse length depends upon R_{14}, R_{16} and the slow turn "off" time of the flip-flop (Figure 5.4-2).

When I_2 exceeds I_{15}, Figure 5.5-1, Q_5 turns "on". In the same fashion, when I_2 falls below I_{15}, Q_5 turns "off". An equivalent circuit model is developed in Figure 5.5-6a which is used to determine the transfer function I_2/V_{in}. The transfer function was solved by a digital computer, and a plot of the results for worst-case conditions is shown in Figure 5.5-4 and Figure 5.5-5. From Figure 5.5-6b,

$$I(s) = \frac{I}{s} = Vo(s)\left[\frac{1}{R_p} + sC_5 + \frac{1}{R_{14} + \frac{1}{sC_6}}\right] \qquad (5.5\text{-}2)$$

and,

$$I_2(s) = \frac{Vo(s)}{R_{14} + \frac{1}{sC_6}} \; . \qquad (5.5\text{-}3)$$

From Figure 5.5-6b,

$$I = \frac{V_{in}}{R_7} \; . \qquad (5.5\text{-}4)$$

Substituting Eq. (5.5-3) and Eq. (5.5-4) into Eq. (5.5-2),

$$I_2(s) = \frac{V_{in}}{R_7 R_{14} C_5} \frac{1}{s^2 + s\left[\frac{1}{\tau_1} + \frac{1}{\tau_2} + \frac{1}{\tau_3}\right] + \frac{1}{\tau_1 \tau_3}} \qquad (5.5\text{-}5)$$

where:

$$\tau_1 = C_5 R_p$$

$$\tau_2 = C_5 R_{14}$$

$$\tau_3 = C_6 R_{14}$$

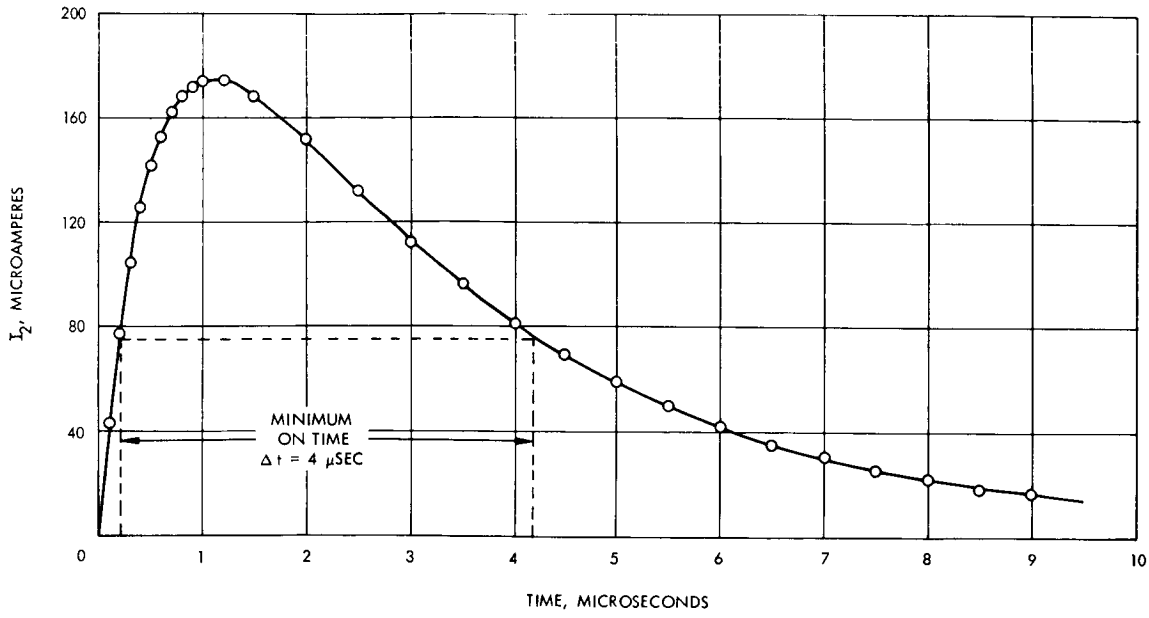


Figure 5.5-4. Transfer function response curve, minimum on time.

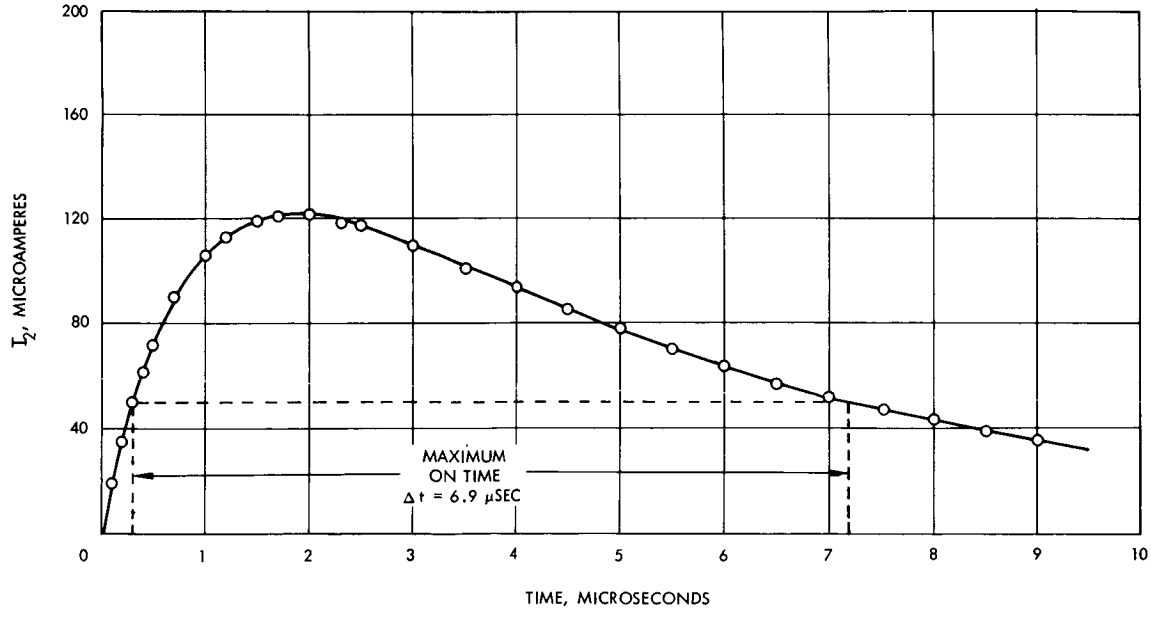


Figure 5.5-5. Transfer function response curve, maximum on time.

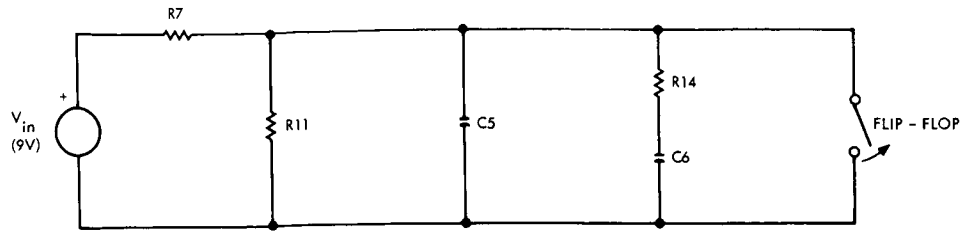


Figure 5.5-6a. Equivalent circuit.

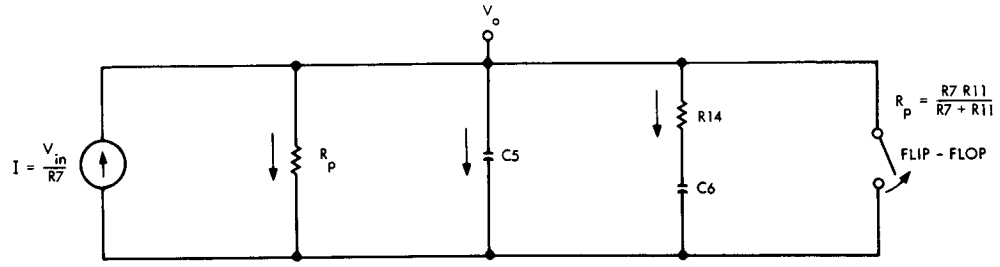


Figure 5.5-6b. Simplified equivalent circuit.

The general inverse Laplace transform of Eq. (5.5-5) is:

$$I_2(t) = k_1 e^{-ts_1} + k_2 e^{-ts_2} \qquad (5.5\text{-}6)$$

where s_1 and s_2 are factors of:

$$s^2 + s\left[\frac{1}{\tau_1} + \frac{1}{\tau_2} + \frac{1}{\tau_3}\right] + \frac{1}{\tau_1 \tau_3} \qquad (5.5\text{-}7)$$

and,

$$k_1 = \frac{V_{in}}{R_7 R_{14} C_5}\left[\frac{1}{s + s_2}\right] s = -s_1 \qquad (5.5\text{-}8)$$

$$k_2 = -k_1 \qquad (5.5\text{-}9)$$

To find the shortest "on" time, all the components are used at their minimum values along with a minimum V_{in}.

Substituting minimum worst-case values into Eq. (5.5-6),

$$I_2(t) = 3.05 \times 10^{-4}\, e^{-3.2981 \times 10^5 t} - 3.05 \times 10^{4}\, e^{-1.91019 \times 10^6 t}. \quad (5.5\text{-}10)$$

Minimum "on" time occurs when the maximum amount of current is shunted through R_{15}.

$$I_{15max} = \frac{V_{be_{5\ max}}}{R_{15\ min}} = 75\ \mu amp \quad (5.5\text{-}11)$$

Base current is supplied to Q_5 when I exceeds I_{15max}. From Figure 5.5-4, it can be seen that the minimum "on" time of Q_5 is 4.0 μsec.

Maximum "on" time is achieved by allowing all the component values and voltage levels to be maximum, and shunting minimum current through R_{15}.

Substituting maximum worst-case values into Equation (5.5-6),

$$I_2(t) = 2.15 \times 10^{4}\, e^{-2.02133 \times 10^5 t} - 2.15 \times 10^{4}\, e^{-1.13787 \times 10^6 t}. \quad (5.5\text{-}12)$$

$$I_{15\ min} = \frac{V_{be_{5\ min}}}{R_{15\ max}} = 50\ \mu amp \quad (5.5\text{-}13)$$

Figure 5.5-5 shows the maximum "on" time to be 6.9 μsec.

Since the maximum discharge time of C_7 is less than the minimum "on" time of Q_5, C_7 will completely discharge under worst-case conditions. That is:

$$\tau_{7max} = 2.58\ \mu sec < 4.0\ \mu sec = \text{minimum "on" time.}$$

C_7 charges at a constant rate by means of the current generator consisting of Q_6 and R_{17}. Figure 5.5-7 is an equivalent circuit for the charging case.

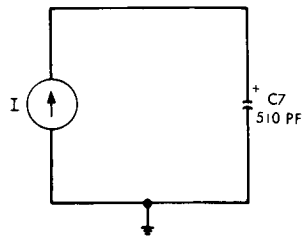


Figure 5.5-7. Equivalent charging circuit.

For a constant current source:

$$I = C \frac{dv}{dt}. \tag{5.5-14}$$

For worst-case charge time:

$$\Delta t_{max} = \frac{C_{7max} \ \Delta V_{max}}{I_{min}}. \tag{5.5-15}$$

Referring to Figure 5.5-1,

$$I_{min} = \frac{E_{1\,min} - V_{be_{6\,max}} - E_{2\,max}}{R_{17max}} = 126\ \mu amp. \tag{5.5-16}$$

$$\Delta V_{max} = 10 \text{ volts}$$

Substituting into Equation (5.5-15),

$$\Delta t_{max} = 42.5\ \mu sec.$$

The minimum time between input pulses at the base of Q_5 is found from the maximum frequency of the astable oscillator (Block 3).

From Equation (5.3-13),

$$f_{max} = 21.9 \text{ kHz} \tag{5.5.-17}$$

f_{max} is divided in half by the bistable (Block 4), therefore,

$$f'_{max} = \frac{f_{max}}{2} = 10.9 \text{ kHz}. \qquad (5.5\text{-}17)$$

The minimum period is:

$$T'_{min} = \frac{1}{f'_{max}} = 92 \,\mu\text{sec}. \qquad (5.5\text{-}18)$$

If the time between pulses, T'_{min}, is greater than the total maximum time that Q_5 is "on", $t_{on\ max}$, and the maximum time it takes to charge C_7, Δt_{max}, then C_7 will completely charge.

If

$$T'_{min} > t_{on\ max} + \Delta t_{max}, \qquad (5.5\text{-}19)$$

then C_7 will have time to completely charge.

$$T_{min} = 92 \,\mu\text{sec} > 59.4 \,\mu\text{sec} = t_{on\ max} + \Delta t_{max}$$

Therefore, C_7 will completely charge under worst-case conditions.

The voltage ramp output is given by the relation

$$\frac{\Delta v}{\Delta t} = \frac{I}{C} \text{ volts/sec} \qquad (5.5\text{-}20)$$

This relation is important in that the duty factor of each phase should be nearly the same. If the ramp rate is decreased then the duty factor will be lengthened and conversely if the ramp rate is increased, the duty factor will decrease.

The maximum ramp voltage is:

$$\left(\frac{\Delta v}{\Delta t}\right)_{max} = \frac{I_{max}}{C_{7\ min}}, \qquad (5.5\text{-}21)$$

where

$$I_{max} = \frac{E_{1\ max} - V_{be\ 6\ min} - E_{2\ min}}{R_{17\ min}} = 152 \,\mu\text{amp}. \qquad (5.5\text{-}22)$$

Therefore,

$$\left(\frac{\Delta v}{\Delta t}\right)_{max} = 0.3 \text{ volts/}\mu\text{sec.}$$

The minimum ramp voltage is given by the relation

$$\left(\frac{\Delta v}{\Delta t}\right)_{min} = \frac{I_{min}}{C_{7\,max}} = 0.235 \text{ volts/}\mu\text{sec.} \qquad (5.5\text{-}23)$$

The duty factor is dependent upon the "on" time of Q5, $(t_1 - t_0)$, and the time required for the ramp voltage to reach the integrator voltage $(t_2 - t_1)$ as shown in Figure 5.5-8.

The maximum period of the DFM output is:

$$T_{max} = (t_1 - t_0)_{max} + (t_2 - t_1)_{max} \qquad (5.5\text{-}24)$$

Figure 5.5-5 shows

$$(t_1 - t_0)_{max} = 6.9 \text{ }\mu\text{sec.}$$

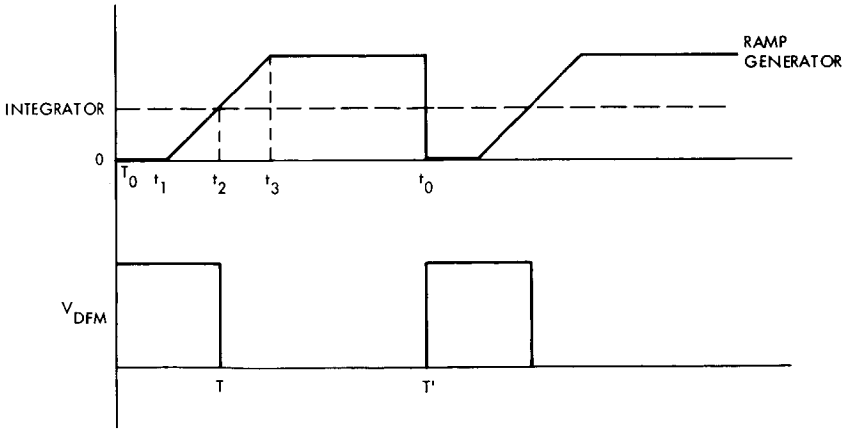


Figure 5.5-8. Duty factor modulator waveforms.

If all reference voltages are made positive for simplification of analysis, then the worst-case integrator voltage, V_{int}, is +5 volts.

$$(t_2 - t_1)_{max} = \frac{V_{int}}{(\Delta v/\Delta t)_{min}} = 21.3\ \mu sec \qquad (5.5\text{-}25)$$

From Eq (5.5-24),

$$T_{max} = 28.2\ \mu sec.$$

The minimum DFM period is:

$$T_{min} = (t_1 - t_0)_{min} + (t_2 - t_1)_{min} \qquad (5.5\text{-}26)$$

Figure (5.5-4) shows

$$(t_1 - t_0)_{min} = 4\ \mu sec$$

$$(t_2 - t_1)_{min} = \frac{V_{int}}{(\Delta v/\Delta t)_{max}} = 16.7\ \mu sec \qquad (5.5\text{-}27)$$

Therefore,

$$T_{min} = 20.7\ \mu sec.$$

The maximum percentage variation per period is:

$$\text{Maximum percent} = \frac{T_{max} - T_{min}}{T'_{min}} = 8 \text{ percent} \qquad (5.5\text{-}28)$$

Since the difference is less than the ten percent required for reliable operation, the ramp generator will work under worst-case conditions. By designing the bistable with pnp transistors, the output pulse (which is coupled to the base of Q_5) would depend on the fast turn-on (instead of turn-off) time characteristics of the bistable transistors. Thus, the on-time of Q_5 could be more tightly controlled.

5.5.2 Worst Case Analysis, Ramp Generator (50-W OCR)

Consideration will now be given to the 50 watt OCR ramp generator. The 250 watt OCR ramp generator is identical in design to the 50 watt generator, Figure 5.5-1. However, analysis varied somewhat, in that a fast rise time signal can be assumed to exist at the input, and R_{17} is changed in value.

The maximum time required to completely discharge C_7, $\tau_{7\ max}$, is the same for both 50 and 250 watt OCR ramp generators.

$$\tau_{7\ max} = 2.58\ \mu sec \qquad (5.5\text{-}1)$$

It is necessary to find the minimum "on" time of Q_5 to insure enough discharge time for C_7. Minimum "on" time occurs when I_2 is minimum and I_{15} is maximum. I_2 (t) is found from the equivalent circuit of Figure 5.5-9b.

From Figure 5.5-9b*,

$$\frac{V_{in} - V_o}{s} = i\ (s) \left[R14 + \frac{1}{sC_6}\right]. \qquad (5.5\text{-}29)$$

Solving for i (t):

$$\mathcal{L}^{-1} i\ (s) = i\ (t) = \frac{V_{in} - V_o}{R_{14}} e^{-\frac{t}{R_{14}C_6}} . \qquad (5.5\text{-}30)$$

Solving for t,

$$t = R_{14}C_6 \ln \frac{V_{in} - V_o}{i\ (t)\ R_{14}} . \qquad (5.5\text{-}31)$$

*A table of critical parameters is given in Table 5.5-2.

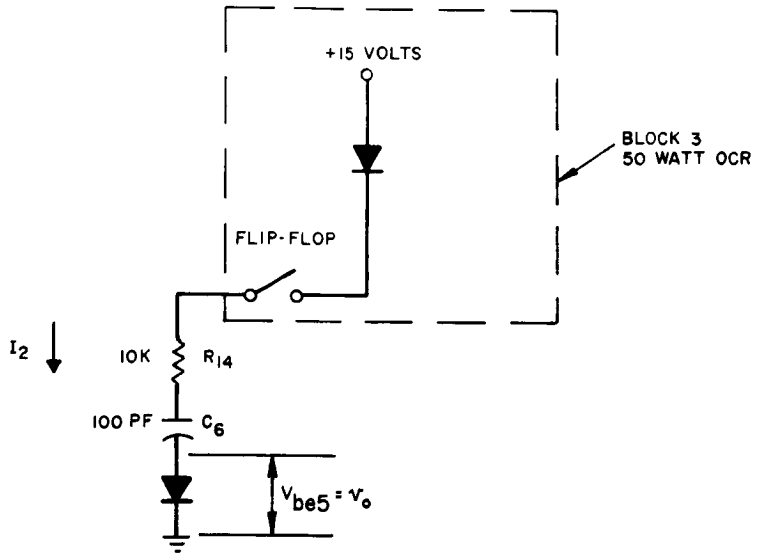


Figure 5.5-9a. Equivalent circuit.

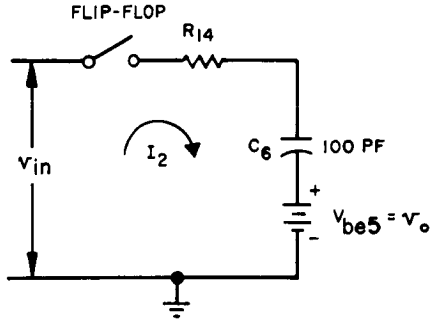


Figure 5.5-9b. Simplified equivalent circuit.

Symbol	Minimum	Maximum
E_1	14.8 volts	15.2 volts
E_2	9.8 volts	10.2 volts
R_{14}	8K original design	12K original design
R_{14}	14.4K suggested design	21.6K suggested design
R_{15}	8K	12K
R_{16}	0.8K	1.2K
R_{17}	42.0K	46.5K
C_6	95 pf	105 pf
C_7	485 pf	535 pf
V_{be_5}	0.6 volt	1 volt
V_{be_6}		0.6 volt

Table 5.5-2. Table of critical parameters (50-W OCR).

Therefore,

$$t_{min} = R_{14\ min}\, C_{6\ min}\, \ln \frac{V_{in\ min} - V_{o\ max}}{i\,(t)_{max}\, R_{14\ min}} \quad . \quad (5.5\text{-}32)$$

Let $i\,(t)_{max}$ be the maximum current in R_{15}.

$$i\,(t)_{max} = \frac{V_{be_{5\ max}}}{R_{15\ min}} = 125\ \mu amp$$

Solving Eq. (5.5-32) yields

$$t_{min} = 1.97\ \mu sec \quad .$$

The minimum "on" time is less than the required time to discharge C_7. Therefore, it is suggested that R_{14} be changed to 18K ±5%. With this change,

$$t_{min} = 2.7\ \mu sec \quad .$$

Sufficient time is now available for C_7 to discharge under worst-case conditions.

Capacitor C_7 will charge at a constant rate. A complete general analysis is found in the 250 watt OCR ramp generator discussion.

From Eq. (5.5-16),

$$I_{min} = 86\ \mu amp \quad .$$

Substituting into Eq. (5.5-15) yields

$$\Delta t_{max} = 62.2\ \mu sec \quad .$$

The minimum time between input pulses is found from the maximum frequency of the astable oscillator (Block 3).

$$T'_{min} = \frac{1}{f_{max}} = 91\ \mu sec\ . \qquad (5.5\text{-}34)$$

If:

$$T'_{min} > t_{on\ max} + \Delta t_{max}, \qquad (5.5\text{-}35)$$

then C_7 will completely charge.

$t_{on\ max}$ = maximum time Q_5 is "on"

From Eq. (5.5-31),

$$t_{on\ max} = R_{14\ max}\, C_{6\ max} \ln \frac{V_{in\ max} - V_{o\ min}}{i(t)_{min}\, R_{14\ max}} \qquad (5.5\text{-}36)$$

$$i(t)\ min = \frac{V_{be_{5\ min}}}{R_{15\ max}} = 50\ \mu amp \qquad (5.5\text{-}37)$$

Therefore,

$$t_{on\ max} = 5.82\ \mu sec\ .$$

From Eq. (5.5-35),

$$91\ \mu sec > 73.8\ \mu sec\ .$$

Therefore, C_7 will completely charge under worst-case conditions.

The duty factor output period variations are found exactly as in the 250 watt OCR case. It was calculated that:

$$(t_1 - t_0)\ max = 5.82\ \mu sec \qquad (5.5\text{-}36)$$

$$(t_2 - t_1)\ max = 28\ \mu sec \qquad (5.5\text{-}25)$$

$$(t_1 - t_0)\ min = 2.7\ \mu sec \qquad (5.5\text{-}32)$$

$$(t_2 - t_1)\ min = 23.1\ \mu sec \qquad (5.5\text{-}27)$$

Component Designation	Type	Rating		Actual Stress	
		Power Dissipation (mw)*		Power Dissipation (mw)*	
Transistor			Vceo (volts)		Vceo (volts)
Q_5	2N2219	800	40	< 1	10
Q_6	2N1132	1 watt	35	< 1	15
Resistors					
R14	10K	250		< 1	
R15 [250w]	10K	250		< 1	
R15 [50w]	18K	250		< 1	
R16	1K	250		< 1	
R17 [250w]	33.2K	125		< 1	
R17 [50w]	44.2K	125		< 1	
Capacitors			(volts)		(volts)
C_6	100pf		500		15
C_7	510pf		500		10

*Unless otherwise noted.

Table 5.5-3. Stress analysis summary for block 5.

Therefore, from Eq. (5.5-24) and Eq. (5.5-26),

$$T_{max} = 33.82\ \mu sec$$
$$T_{min} = 25.8\ \mu sec$$

The maximum percentage variation per period is:

$$\frac{T_{max} - T_{min}}{T'_{min}} = 8.7 \text{ percent} \qquad (5.5\text{-}38)$$

Since this difference is less than the 10 percent maximum variation allowed, the ramp generator will work under worst-case conditions.

5.5.3 Conclusions

If the recommended changes are incorporated into the design, both the 250 watt and 50 watt OCR ramp generators will work under worst-case conditions.

5.5.4 Stress Analysis

A worst-case stress analysis was performed to insure that all components were correctly rated. Table 5.5-3 shows the results of this analysis.

5.6 BLOCK 6, COMPARATOR

The comparator (Figure 5.6-1) senses the integrator voltage level. When the ramp generator develops a voltage which is equal to the integrator voltage, Q_{10} turns "off". A ramp voltage which is negative with respect to the integrator voltage allows Q_{10} to stay "on". The triggering point is ideally at the zero cross-over point. However, due to initial offset in the differential amplifier and current generator fluctuations under worst case, the cross-over point is offset. A maximum offset of 100 millivolts is used as the criterion for worst-case operation.

Two conditions are to be considered.

1. The current generator Q_9 delivers maximum current causing the offset to be on the positive side of zero trigger.

2. The current generator delivers minimum current, such that the offset will be on the negative side of zero trigger.

Figure 6-2 shows the equivalent circuit for the differential amplifier, Q_7 and Q_8 of Figure 5.6-1.

ΔE = offset voltage

Δi_b = offset base current

r_e = intrinsic emitter resistance

Δi_c = offset collector current

β = current gain.

From Figure 5.6-2,

$$\Delta E = \Delta i_b \cdot 2 r_e (1+\beta) \qquad (5.6\text{-}1)$$

$$\Delta i_b = \frac{\Delta i_c}{\beta} \qquad (5.6\text{-}2)$$

$$\Delta i_c = I_{c_8} - I_{c_8}' \qquad (5.6\text{-}3)$$

Where I_{c_8}' is the current required to turn "off" the power amplifier, Q_{10} of Figure 5.6-1.

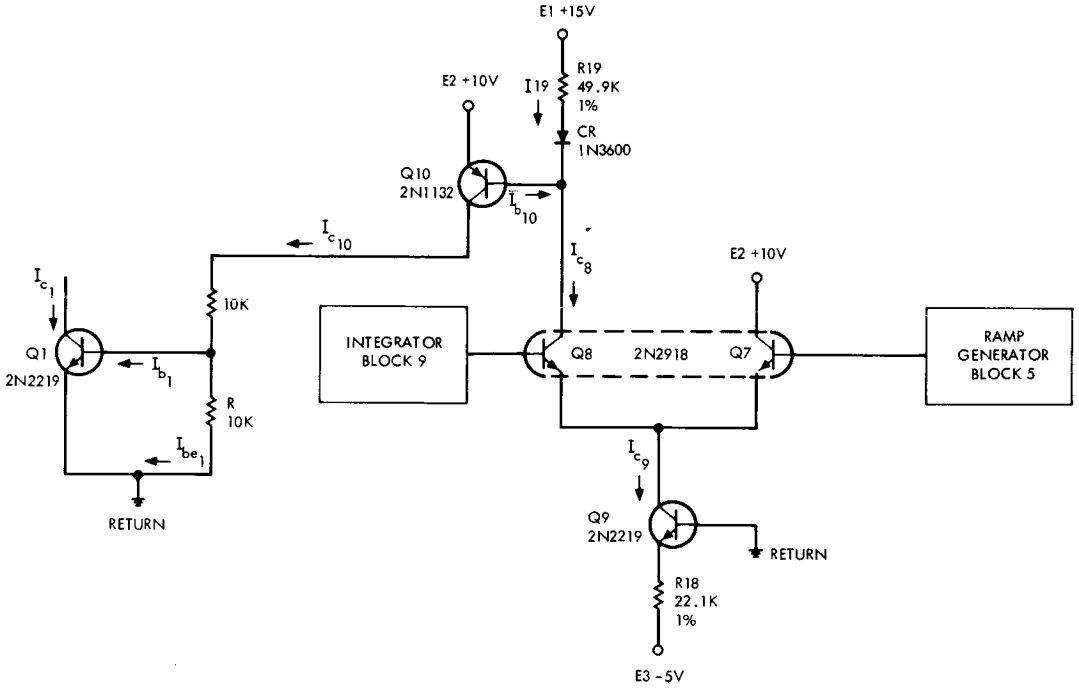


Figure 5.6-1. Comparator.

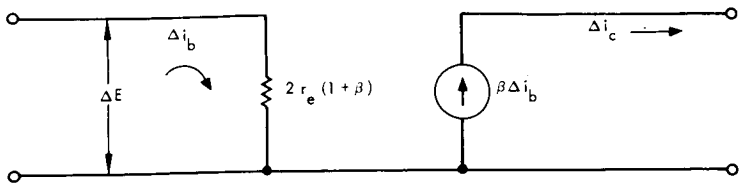


Figure 5.6-2. Differential amplifier equivalent circuit.

Substituting Eq. (5.6-3) and Eq. (5.6-2) into Eq. (5.6-1) and assuming that $\beta \approx 1+\beta$ yields

$$\Delta E = \left(I_{c_8} - I'_{c_8}\right) 2\, r_e \quad . \tag{5.6-4}$$

Considering the first condition,

$$^{*}I_{c_{9\ max}} = \frac{E_{3\ max} - V_{be_{9\ min}}}{R_{18\ min}} = 215\ \mu amp \quad . \tag{5.6-5}$$

From Eq. (5.6-4)

$$\Delta E_{max} = \left(I_{c_{8\ max}} - I'_{c_{8\ min}}\right) 2\, r_{e\ max} \tag{5.6-6}$$

$$I_{c_{8\,max}} = \frac{I_{c_{9\,max}}}{2} = 107.5\ \mu amp \tag{5.6-7}$$

$$r_{e_{max}} \approx \frac{32 \times 10^{-3}}{I_{c_{8\,max}}} = 300\,\Omega \tag{5.6-8}$$

$$I'_{c_{8\,min}} = I_{b_{10\,min}} + I_{19\,min} \tag{5.6-9}$$

---

* A table of critical parameters is found in Table 5.6-2.

Assuming $I_{b_{10\,min}} = 0$ amps, then

$$I_{19\,min} = \frac{E_{1\,min} - E_{2\,max} - V_{be_{10\,max}} + V_{CR\,min}}{R_{19\,max}} = 92\ \mu amp \qquad (5.6\text{-}10)$$

From Eq. (5.6-9)

$$I'_{c_{8\,min}} = 92\ \mu amp\ .$$

Substituting into Equation (5.6-6) yields

$$\Delta E_{max} = 9.35\ mv\ offset$$

If ΔE_o is the initial offset of the difference amplifier, the total offset is:

$$\Delta E_T = \Delta E_{max} + \Delta E_{o\,max} = 19.35\ mv\ . \qquad (5.6\text{-}11)$$

The second condition occurs when the current generator delivers minimum current.

From Eq. (5.6-4),

$$\Delta E_{min} = \left(I_{c_{8\,min}} - I'_{c_{8\,max}}\right) 2\, r_{e\,max} \qquad (5.6\text{-}12)$$

$$I_{c_{9\,min}} = \frac{E_{3\,min} - V_{be_{9\,max}}}{R_{18\,max}} = 186\ \mu amp \qquad (5.6\text{-}13)$$

$$I_{c_{8\,min}} = \frac{I_{c_{9\,min}}}{2} = 93\ \mu amp \qquad (5.6\text{-}14)$$

$$r_{e\,max} = \frac{32}{I_{c_{8\,min}}} = 345\ \Omega \qquad (5.6\text{-}15)$$

$$I'_{c_{8\ max}} = I_{b_{10\ max}} + I_{19\ max} \tag{5.6-16}$$

$$I_{19\ max} = \frac{E_{1\ max} - E_{2\ min} - V_{be_{10\ min}} + V_{CR\ max}}{R_{19\ min}} = 110\ \mu amp \tag{5.6-17}$$

Figure 5.6-3 is the equivalent circuit for finding $I_{b_{10\ max}}$.

From Figure 5.6-3.

$$I_{b_{10\ max}} = \frac{I_{c_{10\ max}}}{\beta_{10\ min}} \tag{5.6-18}$$

$$I_{c_{10\ max}} = I_{b_{1\ max}} + I_{be_{1\ max}} \tag{5.6-19}$$

$$I_{b_{1\ max}} = \frac{I_{c_{1\ max}}}{\beta_{1\ min}} = 98\ \mu amp \tag{5.6-20}$$

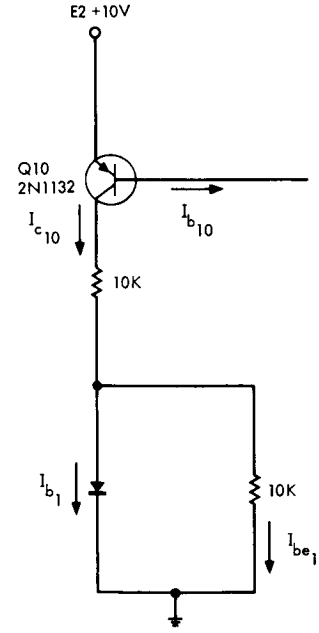


Figure 5.6-3. Equivalent circuit.

It has been shown in the switching circuit analysis that $I_{c_{1\,max}}$ = 5.885 ma.

$$I_{be_{1max}} = \frac{V_{be_{1\,max}}}{R_{min}} = 75\ \mu amp \qquad (5.6\text{-}21)$$

Substituting into equation (5.6-18) yields

$$I_{b_{10\,max}} = 17.3\ \mu amp\ .$$

Substituting $I_{b10\,max}$ and $I_{19\,max}$ into Equation (5.6-16) yields

$$I'_{c_{8\,max}} = 127.3\ \mu amp\ .$$

Therefore,

$$\Delta E_{min} = -21.9\ mv.$$

From Eq. (5.6-11),

$$\Delta E_T = \Delta E_{min} + \Delta E_{o\,min} = -31.9\ mv\ . \qquad (5.6\text{-}17)$$

5.6.1 Conclusions

Figure 5.6-4 is a graphical interpretation of the results. Since the maximum offset does not exceed the 100 millivolt limit, the difference amplifier and power amplifier will work under worst-case conditions.

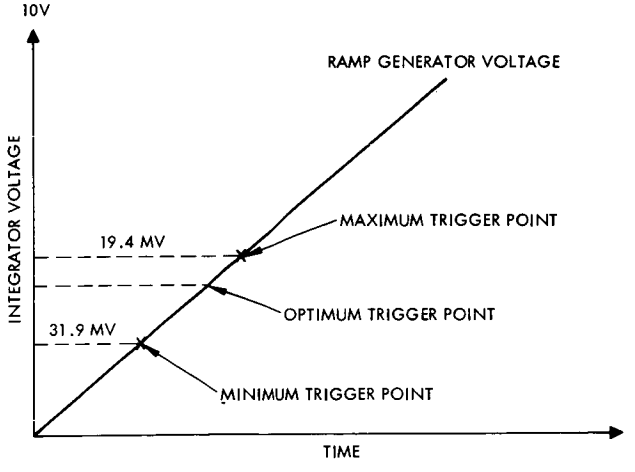


Figure 5.6-4. Maximum and minimum trigger levels.

5.6.2 Stress Analysis

A stress analysis was performed on the differential amplifier to insure that all of the components were not over stressed. The results of this analysis are found in Table 5.6-1.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation (mw)*			Power Dissipation (mw)*		
Transistors			Vceo (volts)			Vceo (volts)	
Q_7, Q_8	2N2918	250	45		<1	10	
Q_9	2N2219	800	40		1	5	
Q_{10}	2N1132	1 watt	35		2	10	
Resistors							
R_{18}	22.1K	125			1		
R_{19}	49.9K	125			<1		
			PIV	I_f		PIV	I_f
Diodes			(volts)	(ma)		(volts)	(ma)
CR	1N3600	500	50	200		0	0.2

*Unless otherwise noted.

Table 5.6-1. Stress analysis summary for block 6.

Symbol	Minimum	Maximum
E_1	14.9 volts	15.1 volts
E_2	9.9 volts	10.1 volts
E_3	-4.9 volts	-5.1 volts
R	8K	
R_{18}	21K	23.2K
R_{19}	47.5K	52.1K
V_{CR}	0.6 volt	0.6 volt
β_1	60	
β_{10}	10	
$V_{be_{10}}$	0.6 volt	0.6 volt
V_{be_9}	0.6 volt	0.6 volt
ΔE_o	10 mv	10 mv
V_{be_1}		0.6 volt

Table 5.6-2. Table of critical parameters for block 6.

5.7 BLOCK 7, PEAK HOLDING COMPARATOR

This circuit (Figure 5.7-1) acts as a memory to store a voltage proportional to the maximum current delivered to the battery. When the current drops a preset amount below the maximum point, the circuit generates a pulse which is then used to trigger the bistable.

A 250 Hz signal with a peak of approximately one volt (Figure 5.7-2a) is the input to the peak holding comparator. The operation is as follows: Assume C_1 is charged to minus five volts. As the input voltage increases, Q_1 is "on" and Q_2 is "off." C_1 charges to the peak input voltage. As the input decreases, the diode, CR_1,

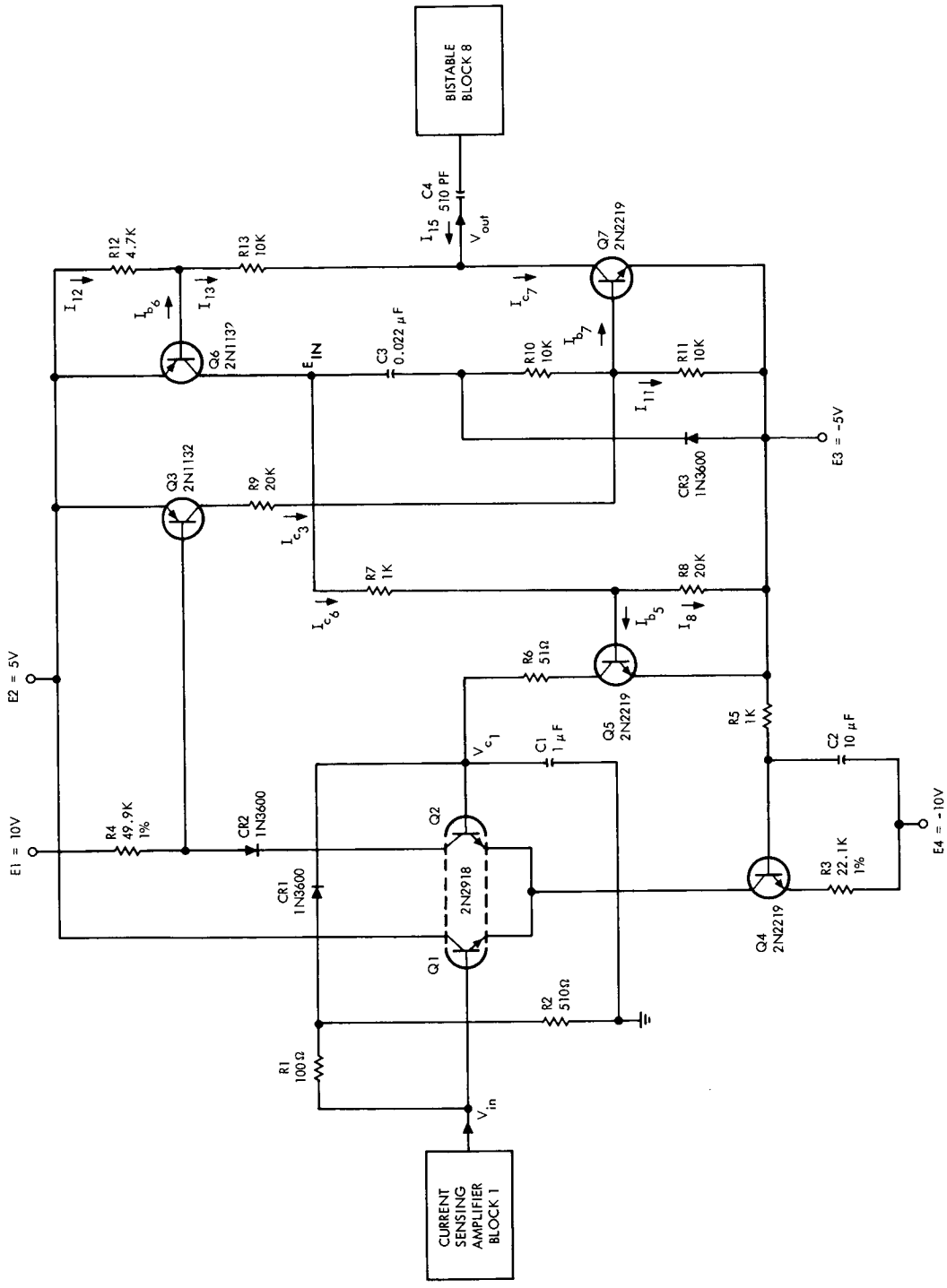


Figure 5.7-1. Peak holding comparator (block 8).

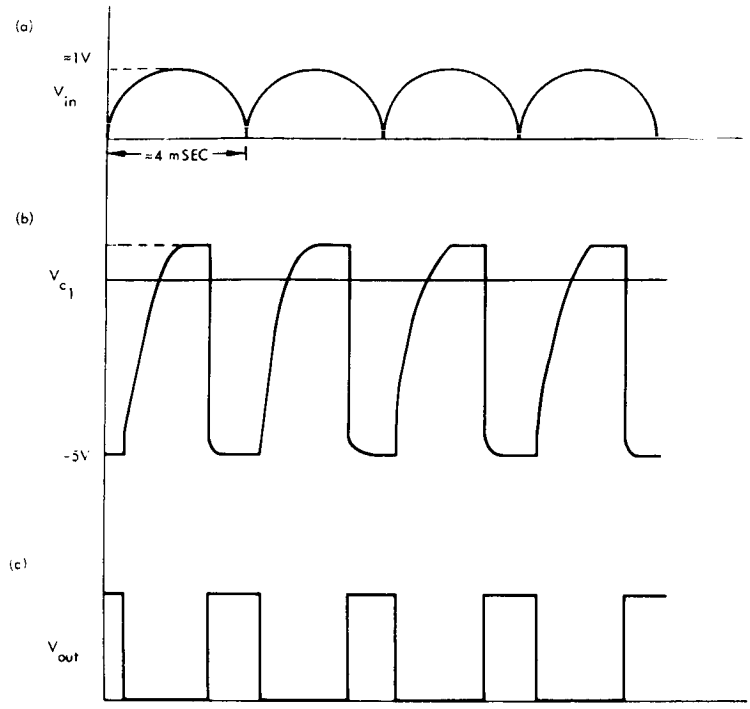


Figure 5.7-2. Peak holding comparator waveforms.

becomes back biased turning Q_2 "on," which turns Q_7 "on." A negative pulse is delivered to the bistable, and Q_6 is turned "on" which causes Q_5 to turn "on." Capacitor C_1 charges to minus five volts turning Q_2 "off."

When Q_2 turns "off," the same sequence described above, turns Q_5 "off." The cycle is now ready to begin again.

Two criteria are necessary to insure circuit operation.

1. The total offset required to turn "on" Q_3 is not to exceed 0.3 volts.
2. C_1 must have sufficient time to charge to minus five volts, yet Q_5 must be "off" when the next cycle begins.

The maximum offset required to turn Q_3 "on" is defined by the following equation:

$$\Delta E''_{max} = \Delta E_{Tmax} + \Delta E_{R_{1,\ 2\ max}}, \qquad (5.7\text{-}1)$$

where

$\Delta E_{T_{max}}$ is the total offset introduced by the difference amplifier,

and

$\Delta E_{R_{1,\,2\ max}}$ is the offset due to the voltage divider network,

R_1 and R_2.

Figure 5.7-3 is the equivalent circuit for finding ΔE max.

$$\Delta E_T = \Delta E + \Delta E' \tag{5.7-2}$$

where

$\Delta E'$ = the initial offset characteristic of the device.

From Figure 5.7-3 (b),

$$\Delta E_{max} = \Delta I_{b_{max}} \cdot 2 r e_{max} (1+\beta) \tag{5.7-3}$$

assuming

$$\beta \approx (1+\beta), \tag{5.7-4}$$

then

$$\Delta I_{b_{max}} (1+\beta) \approx \Delta I_{c_{2\ max}} . \tag{5.7-5}$$

Therefore,

$$\Delta E_{max} \approx 2 r_{e_{max}} \Delta I_{c_{2\ max}} . \tag{5.7-6}$$

From Figure 5.7-3 (a),

$$I_{c_{2\ max}} = \left(I_{4\ max} + I_{b_{3\ max}} \right) - I_{c_{2\ min}} \tag{5.7-7}$$

$$I_{c_{2\ min}} = \frac{I_{c_{4\ min}}}{2} = 95\ \mu amp \tag{5.7-8}$$

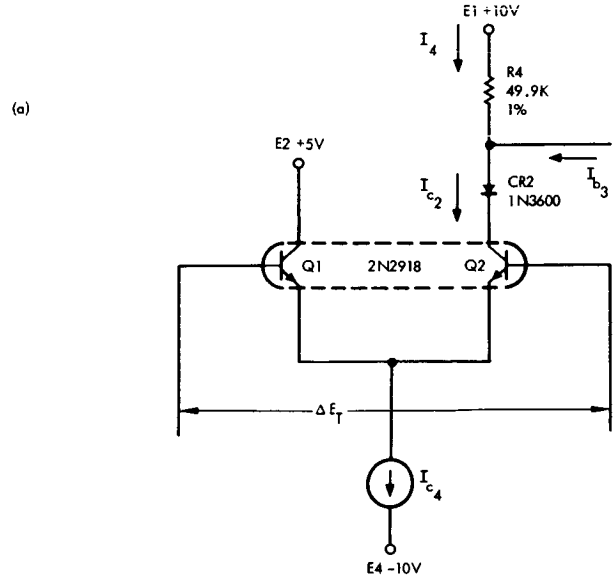


Figure 5.7-3a. Reduced model for difference amplifier.

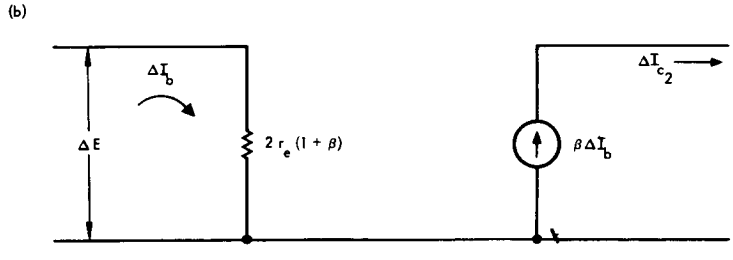


Figure 5.7-3b. Difference amplifier equivalent circuit.

where

$$^{*}I_{c_{4\,min}} = \frac{E_3 - E_4 - V_{be_{4\,max}}}{R_{3\,max}} = 189\mu\,amp \qquad (5.7\text{-}9)$$

$$I_{b_{3\,max}} = \frac{I_{c_{3\,max}}}{\beta_{3\,min}} \qquad (5.7\text{-}10)$$

$$I_{c_{3\,max}} = I_{11\,max} + I_{b_{7\,max}} \qquad (5.7\text{-}11)$$

$$I_{b_{7\,max}} = \frac{I_{c_{7\,max}}}{\beta_{7\,min}} \qquad (5.7\text{-}12)$$

$$I_{c_{7\,max}} = I_{15\,max} + I_{13\,max} \qquad (5.7\text{-}13)$$

$$I_{13\,max} = I_{b_{6\,max}} + I_{12\,max} \qquad (5.7\text{-}14)$$

$$I_{b_{6\,max}} = \frac{I_{c_{6\,max}}}{\beta_{6\,min}} \qquad (5.7\text{-}15)$$

$$I_{c_{6\,max}} = I_{b_{5\,max}} + I_{8\,max} \qquad (5.7\text{-}16)$$

$$I_{b_{5\,max}} = \frac{I_{c_{5\,max}}}{\beta_{5\,min}} \qquad (5.7\text{-}17)$$

*A table of critical parameters is found in Table 5.7-2.

$$I_{c_{5\ max}} = \frac{V_{C_{1\ max}} - E_{3\ max}}{R_{6\ min}} = 150\ ma \quad (5.7\text{-}18)$$

$$I_{8\ max} = \frac{V_{be_{5\ max}}}{R_{8\ min}} = 3.75\ \mu amp \quad (5.7\text{-}19)$$

From Eq. (5.7-17),

$$I_{b_{5\ max}} = 7.5\ ma\ .$$

Substituting into Eq. (5.7-16) and Eq. (5.7-15) yields

$$I_{c_{6\ max}} = 7.5\ ma$$

$$I_{b_{6\ max}} = 940\ \mu amp$$

$$I_{12\ max} = \frac{V_{be_{6\ max}}}{R_{12\ min}} = 213\ \mu amp \quad (5.7\text{-}20)$$

From Eq. (5.7-14),

$$I_{13\ max} = 1.153\ ma\ .$$

Figure 5.7-4 is the circuitry which delivers I_{15}.

From Figure 5.7-4,

$$I_{15\ max} = \frac{E_{2\ max} - E_{3\ max} - V_{ce_{7\ min}}}{R_{p\ min}} = 1.87\ ma \quad (5.7\text{-}21)$$

where

$$R_{p\,min} = R_{14_{min}} // R_{15_{min}} // R_{16_{min}} = 5.33K \quad (5.7\text{-}22)$$

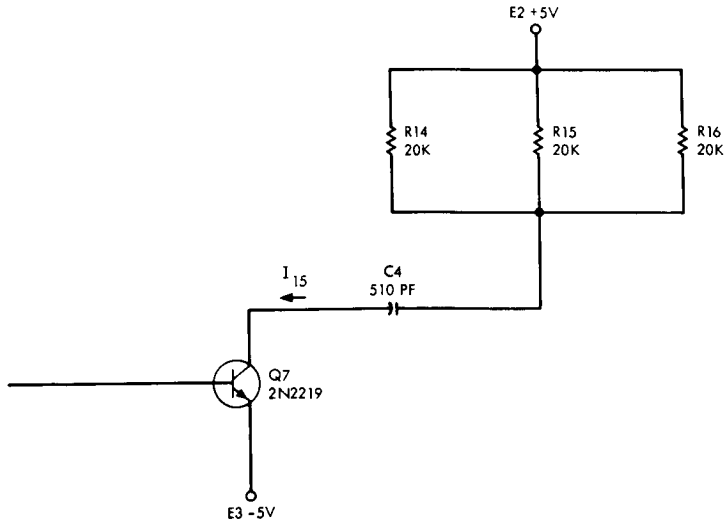


Figure 5.7-4. Equivalent circuit.

Therefore, from Eq. (5.7-13) and Eq. (5.7-12)

$$I_{c_{7\ max}} = 3.02\ ma$$

$$I_{b_{7\ max}} = 100\ \mu amp$$

$$I_{11\ max} = \frac{V_{be_{7\ max}}}{R_{11\ min}} = 75\ \mu amp \qquad (5.7\text{-}23)$$

Substituting into Eq. (5.7-11) and Eq. (5.7-10) yields

$$I_{c_{3\ max}} = 175\ \mu amp$$

$$I_{b_{3\ max}} = 8.75\ \mu amp \qquad (5.7\text{-}24)$$

From Figure 5.7-3 (a),

$$I_{4\ max} = \frac{E_{1\ max} - E_{2\ min} + V_{be_{3\ min}}}{R_{4\ min}} = 110\ \mu amp \qquad (5.7\text{-}25)$$

Substituting into Eq. (5.7-7) yields

$$\Delta I_{c_{2\ max}} = 23.75\ \mu amp\ .$$

From Eq. (5.7-8),

$$r_{e_{max}} \cong \frac{30}{I_{c_{2\ min}}\ ma} = 315\ \Omega\ . \qquad (5.7\text{-}26)$$

From Eq. (5.7-6),

$$\Delta E'_{max} = 14.8\ mv\ .$$

Therefore, from Eq. (5.7-2),

$$\Delta E_T = 24.8\ mv\ .$$

Figure 5.7-5 is the equivalent circuit model for finding $\Delta E_{R_{1,2\ max}}$.

Laboratory tests show that zero drop can be assumed across CR_1.

$$\Delta E_{R_{1,2\ max}} = E_{in\ max} - V_{min} \qquad (5.7\text{-}27)$$

From Figure 5.7-5,

$$V_{min} = E_{in\ max} \frac{R_{2\ min}}{R_{2\ min} + R_{1\ max}} = 0.775\ volts. \qquad (5.7\text{-}28)$$

Therefore,

$$\Delta E_{R_{1,2\ max}} = 225\ mv\ .$$

From Eq. (5.7-1)

$$\Delta E''_{max} = 249.8\ mv$$

$$\Delta E''_{min} = \Delta E_{T\ min} + \Delta E_{R_{1,2\ min}} \qquad (5.7\text{-}29)$$

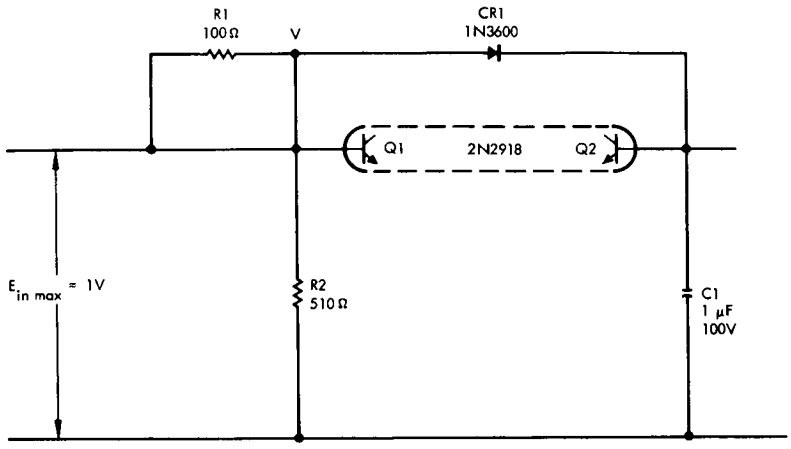


Figure 5.7-5. Model for finding $E_{R_{1,\ 2\ max}}$.

Let

$$\Delta E_{T\ min} = 0 \text{ volts} .$$

$$\Delta E_{R_{1,2\ min}} = E_{in\ max} - V_{max} = 130 \text{ mv} \qquad (5.7\text{-}30)$$

where

$$V_{max} = E_{in\ max} \frac{R_{2\ max}}{R_{2\ max} + R_{1\ min}} = 870 \text{ mv} . \qquad (5.7\text{-}31)$$

From Equation (5.7-29),

$$\Delta E''_{min} = 130 \text{ mv} .$$

Since the maximum offset is less than 300 millivolts it is evident that the first criterion has been satisfied.

The time necessary for C_1 to charge to minus five volts is:

$$T = 4\, R_6 C_1 \qquad (5.7\text{-}32)$$

It is assumed that four time constants will allow C_1 to charge to minus five volts.

The maximum time required is:

$$T_{max} = 4\, R_{6\ max}\, C_{1\ max} = 256\ \mu sec\ . \qquad (5.7\text{-}33)$$

The "on" time of Q_5, T_5, determines the charging time for C_1. From Figure 5.7-1 it can be seen that the "on" time of Q_5 is directly dependent upon the "on" time, T_7, of Q_7.

Therefore C_1 will charge to minus five volts if:

$$T_{7\ min} \geq T_{5\ max} \qquad (5.7\text{-}34)$$

Figure 5.7-6 (b) is the equivalent circuit for finding T_7. Q_7 will turn "on" when $I_{10} > I_{11}$.

Solving for $I_{10}(s)$ yields

$$I_{10}(s) = \frac{E_{in}}{sR_{10}} \frac{1}{s + \frac{1}{R_{10}C_3}} \qquad (5.7\text{-}35)$$

$$\mathcal{L}^{-1} I_{10}(s) = I_{10}(t) = \frac{E_{in}}{R_{10}} e^{-\frac{t_7}{R_{10}C_3}} \qquad (5.7\text{-}36)$$

Solving for t yields

$$t_7 = R_{10}\, C_3 \ln \frac{E_{in}}{I_{10}(t_7) R_{10}}\ . \qquad (5.7\text{-}37)$$

Solving for T_7 min yields

$$T_{7\ min} = R_{10\,min}\, C_{3\,min} \ln \frac{E_{in\ min}}{I_{10}(t)_{max} R_{10\ min}}\ . \qquad (5.7\text{-}38)$$

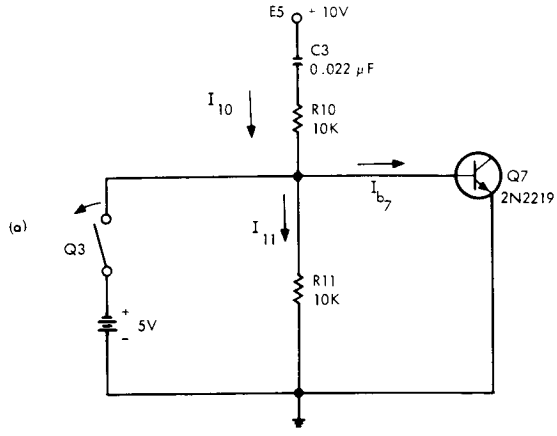


Figure 5.7-6a. Reduced model.

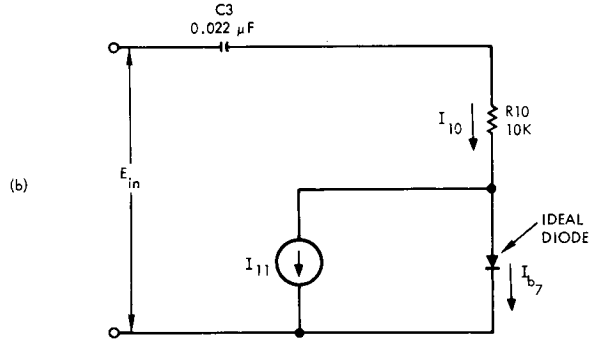


Figure 5.7-6b. Reduced model equivalent circuit.

From Figure 5.7-1,

$$E_{in\ min} = E_{2\ min} - E_{3\ min} - V_{ce_{6\ max}} - V_{be_{7\ max}} = 9 \text{ volts} . \quad (5.7\text{-}39)$$

From Figure 5.7-6 (b), Q_7 will turn "off" when $I_{10} = I_{11}$. Therefore, let $I_{10\ max} = I_{11\ max}$.

$$I_{11\ max} = \frac{V_{be_{7\ max}}}{R_{11\ min}} = 75 \ \mu amp \quad (5.7\text{-}40)$$

Substituting into Equation (5.7-38) yields

$$T_{7\ min} = 465 \ \mu sec .$$

From Equation (5.7-34), (5.7-41)

$$T_{7\ min} = 465 \ \mu sec > 265 \ \mu sec = T_{5\ max} .$$

Therefore, C_1 will charge to minus five volts under worst-case conditions.

Q_5 will turn "off" before the next cycle if

$$T_{7\ max} < \frac{T_p}{2} , \quad (5.7\text{-}42)$$

where T_p = period of the input signal V_{in} Figure 5.7-2 (a).

$$\frac{1}{2} T_p = 2{,}000 \ \mu sec$$

From Equation (5.7-37),

$$T_{7\ max} = R_{10\ max} C_{3\ max} \ln \frac{E_{in\ max}}{I_{10\ (t)_{min}} R_{10\ max}} \quad (5.7\text{-}43)$$

$$E_{in\ max} = E_{2\ max} - E_{3\ max} - V_{ce_{6\ min}} - V_{be_{7\ min}} = 9.4 \text{ volts} \quad (5.7\text{-}44)$$

$$I_{10}(t)_{min} = I_{11}(t)_{min} = \frac{V_{be_{7\,min}}}{R_{11\ max}} = 50\ \mu\text{amp} \quad (5.7\text{-}45)$$

Substituting into Equation (5.7-43) yields

$$T_{7\ max} = 760\ \mu\text{sec} .$$

From Equation (5.7-42),

$$T_{7\ max} = 760\ \mu\text{sec} < 2,000\ \mu\text{sec} = \frac{1}{2} T_p . \quad (5.7\text{-}46)$$

Therefore, Q_5 will turn "off" before the next cycle under worst-case conditions.

5.7.1 Conclusion

The peak holding comparator will work under worst-case conditions.

5.7.2 Stress Analysis

A stress analysis was performed to insure that no component was over-stressed. The results can be found in Table 5.7-1.

5.8 BLOCK 8, BISTABLE

This block is identical to block 4, therefore the analysis is the same.

5.8.1 Conclusions

The bistable will operate under worst-case conditions. It is suggested that the speed-up capacitors be changed to 300 pf.

Component Designation	Type	Rating		Actual Stress	
		Power Dissipation (mw)*		Power Dissipation (mw)*	
Transistors			Vceo (volts)		Vceo (volts)
Q_1 and Q_2	2N2918	250	45	1	6
Q3	2N1132	1 watt	-35	1	-10
Q4	2N2219	800	40	1	10
Q5	2N2219	800	40	23 max	6
Q6	2N1132	1 watt	-35	75 max	10
Q7	2N2219	800	40	30.2 max	10
Resistors					
R_1	100Ω	250		60	
R_2	510Ω	250		32	
R_3	22.1K	125		1	
R_4	49.9K	125		2	
R_5	1K	250		<1	
R_6	51Ω	250		80	
R_7	1K	250		7	
R_8	20K	250		<1	
R_9	20K	250		1	
R_{10}	10K	250		10	
R_{11}	10K	250		<1	
R_{12}	4.7K	250		<1	
R_{13}	10K	250		1	

*Unless otherwise noted.

Table 5.7-1. Stress analysis summary for block 7.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation (mw)*			Power Dissipation (mw)*		
			PIV (volts)	I_f (ma)		PIV (volts)	I_f (ma)
Diodes							
CR_1	1N3600	500	50	200	30	1	50
CR_2	1N3600	500	50	200	<1	0	0.2
CR_3	1N3600	500	50	200	<1	10	≈0
Capacitors			(volts)			(volts)	
C_1	1μf		100			5	
C_2	10μf		15		30.2 max	1	
C_3	0.022μf		100			10	
C_4	510pf		500			10	
*Unless otherwise noted.							

Table 5.7-1 (continued). Stress analysis summary for block 7.

Symbol	Minimum	Maximum
E_1	9.9 volts	10.1 volts
E_2	4.9 volts	5.1 volts
E_3	-4.9 volts	-5.1 volts
E_4	-9.9 volts	-10.1 volts
R_1	80 Ω	120 Ω
R_2	408 Ω	610 Ω
R_3		23.3K
R_4	47K	
R_6	40.8 Ω	61 Ω
R_7	0.8K	1.2K
R_8	16K	
R_{10}	8K	12K
R_{11}	8K	12K
R_{12}	3.75K	
R_{13}	8K	12K
R_{14}	16K	
R_{15}	16K	
R_{16}	16K	
β_3	20	
V_{be_3}	0	
V_{be_4}		0.6 volt
β_5	20	
V_{be_5}		0.6 volt

Table 5.7-2. Table of critical parameters for block 7.

Symbol	Minimum	Maximum
β_6	8	
V_{be_6}		0.8 volt
V_{ce_6}	0 volt	0.2 volt
β_7	30	
V_{be_7}	0.6 volt	0.6 volt
$\Delta E'$		10 mv
V_{C_1}		1 volt

Table 5.7-2 (continued). Table of critical parameters for block 7.

5.9 BLOCK 9, INTEGRATOR

The bistable multivibrator, block 8, drives an operational amplifier with capacitive feedback as shown in Figures 5.9-1 and 5.9-2. This feedback acts to integrate the bistable output. Figure 5.9-3 represents the integrator input and output waveforms.

It is necessary to determine the maximum and minimum ramp rates of the integrator output. These rates are used for the worst-case analysis of the level detector, block 11.

From Figure 5.9-2,

$$E_o = \frac{E_{in}}{R_{in} C_1} t = kt \qquad (5.9\text{-}1)$$

where

K = the slope of the integrator output in volts per second.

Consider:

1. K^+_{max} and K^+_{min} for a positive bistable input.
2. K^-_{max} and K^-_{min} for a negative bistable input.

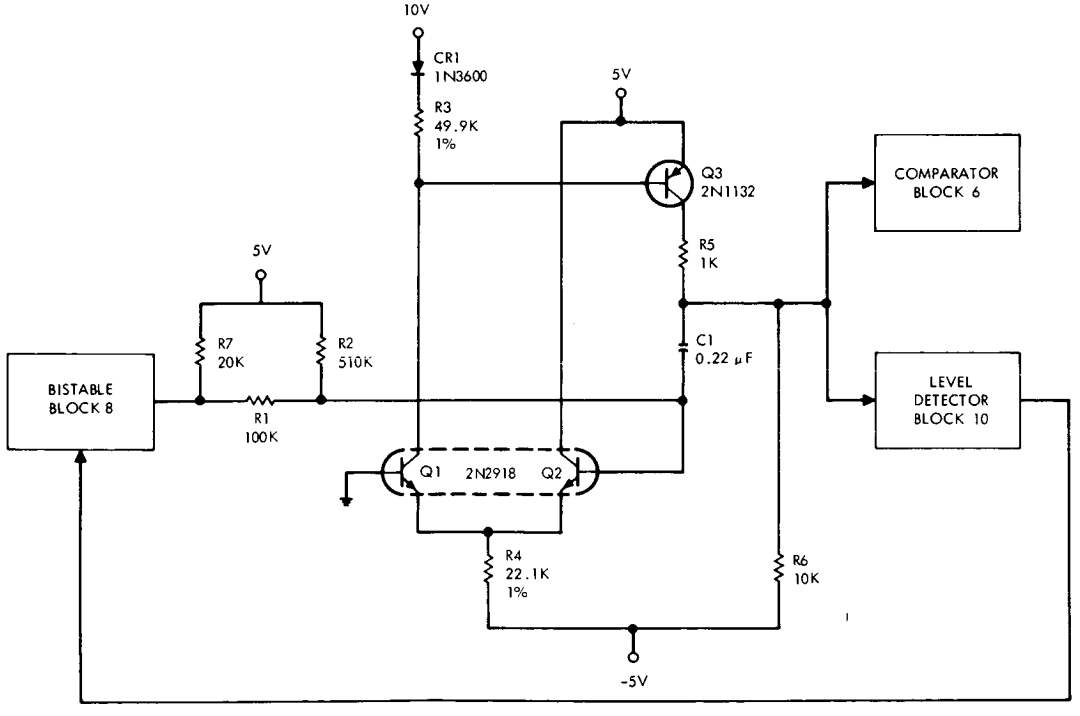


Figure 5.9-1. Integrator.

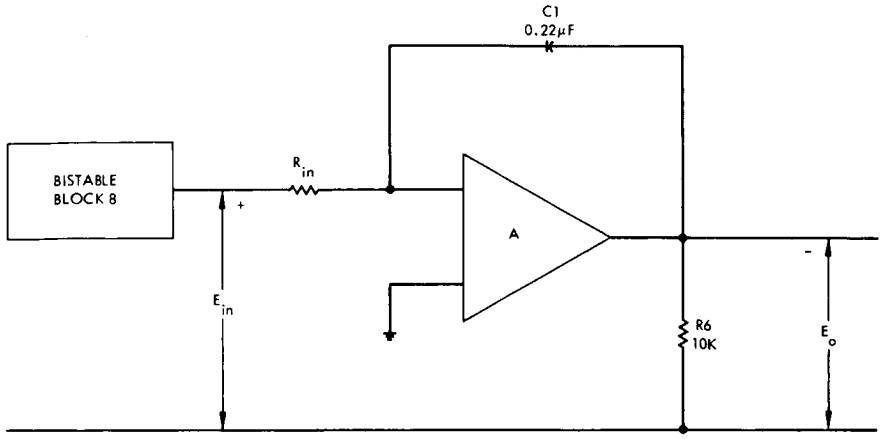


Figure 5.9-2. Integrator model.

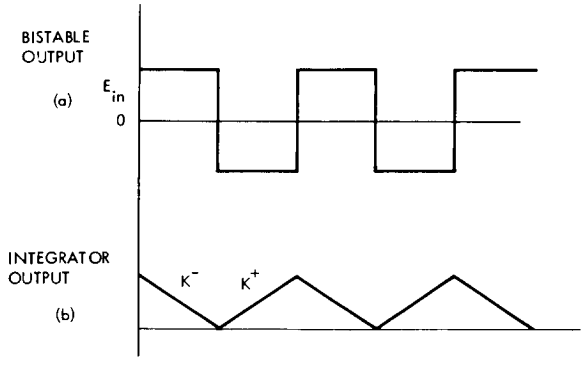


Figure 5.9-3. Bistable and integrator waveforms.

From Eq. (5.9-1),

$$K_{max} = \frac{E_{in\ max}}{R_{in\ min} C_{1\ min}} \qquad (5.9\text{-}2)$$

$$K_{min} = \frac{E_{in\ min}}{R_{in\ max} C_{1\ max}} \qquad (5.9\text{-}3)$$

Considering the first case:

$$^{*}R_{in\ min} = (R_{7\,min} + R_{1\ min}) // R_{2\,min} = 78K \qquad (5.9\text{-}4)$$

$$R_{in\ max} = (R_{7\,max} + R_{1\ max}) // R_{2\,max} = 116K \qquad (5.9\text{-}5)$$

Substituting into Eq. (5.9-2) yields

$$K^{+}_{max} = 310 \text{ volts/sec} \qquad (5.9\text{-}6)$$

$$K^{+}_{min} = 182 \text{ volts/sec} \qquad (5.9\text{-}7)$$

Considering the second case:

$$R_{in\ min} = R_{1\,min} // R_{2\ min} \qquad (5.9\text{-}8)$$

$$R_{in\ max} = R_{1\ max} // R_{2\ max} \qquad (5.9\text{-}9)$$

Substituting into Eq. (5.9-3) yields

$$K^{-}_{max} = -363 \text{ volts/sec} \qquad (5.9\text{-}10)$$

$$K^{-}_{min} = -210 \text{ volts/sec} \qquad (5.9\text{-}11)$$

5.9.1 Stress Analysis

A stress analysis was performed to insure proper stress levels on all components. The results of this analysis are found in Table 5.9-2.

---

*A table of critical parameters is found in Table 5.9-1.

Symbol	Minimum	Maximum
E_{in}	4.9 volts	5.1 volts
R_1	80K	120K
R_2	408K	610K
R_7	16K	24K
C_1	0.21μf	0.232μf

Table 5.9-1. Table of critical parameters for block 9.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation (mw)*			Power Dissipation (mw)*		
Transistors			Vceo (volts)			Vceo (volts)	
Q_1 and Q_2	2N2918	250	45		<1	15	
Q_3	2N1132	1 watt	-35		4	-6	
Resistors							
R_1	100K	250			<1		
R_2	510K	250			<1		
R_3	49.9K	125			<1		
R_4	22.1K	125			<1		
R_5	1K	250			9		
R_6	10K	250			2		
R_7	20K	250			<1		
Diodes			PIV (volts)	I_f (ma)		PIV (volts)	I_f (ma)
CR_1	1N3600	500	50	200	<1	0	0.1
Capacitors			(volts)			(volts)	
C_1	(0.22)μf		100			10	

*Unless otherwise noted.

Table 5.9-2. Stress analysis summary for block 9.

5.10 BLOCK 10, LEVEL DETECTOR

The level detector (Figure 5.10-1) constrains the OCR to track the maximum power point. Without this level detector logic, it was found that turn-on conditions, load transients, and power transients would cause the OCR to operate about a point other than the maximum power point.

The level detector operates in the following manner. Under normal operating conditions, the integrator output has a limited voltage range as shown in Figure 5.9-3 (b). When the OCR tends to move too far from the maximum power point, the integrator output voltage extends beyond its normal range. The amplifier Q_3 and Q_4, detects the abnormal range and turns on either Q_1 or Q_2 depending upon the integrator slope. A pulse is delivered to one side of the flip-flop causing it to change state. This in turn forces the integrator to reverse its direction. Operation is now brought back to the maximum power tracking state. Under normal conditions, the level detector has no function.

Two worst-case criteria must be met for satisfactory operation.

1. The current generator, Q_5, should not saturate under worst-case integrator input.
2. Transistors Q_1 and Q_2 should trip only after normal integrator voltages have been exceeded.

Figure 5.10-2 is a model for the current source. The current source will remain in the active region if:

$$V_{c_{min}} > V_{b_{max}} - V^{*}_{be_{5\ min}} \qquad (5.10\text{-}1)$$

$$V_{c_{min}} = V_{in\ min} - V_{be_{3\ max}} - I_{c\ max} R_{6\ max} \qquad (5.10\text{-}2)$$

$$I_{c_{max}} \approx I_{9\ max} = \frac{V_{b\ max} - V_{be_{5\ min}}}{R_{9\ min}} \qquad (5.10\text{-}3)$$

$$V_{b\ max} = E_{1\ max} - R_{8\ min} I_{8\ min} = 2.8 \text{ volts} \qquad (5.10\text{-}4)$$

*A table of critical parameters is found in Table 5.10-1.

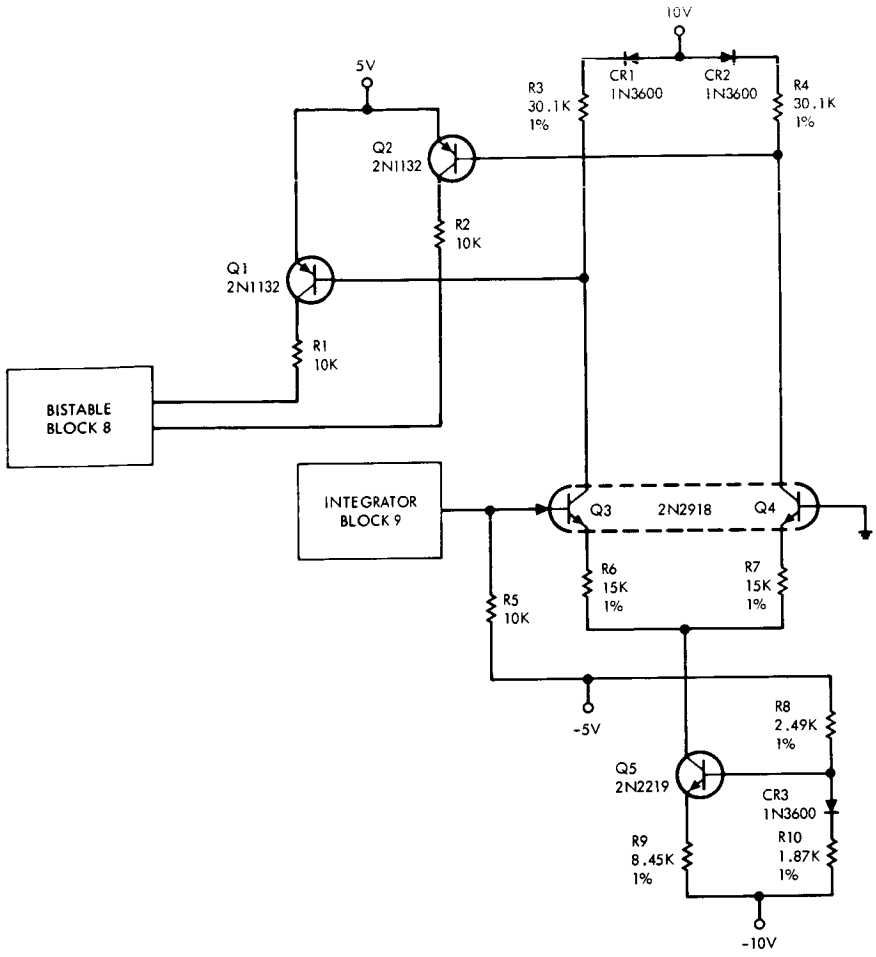


Figure 5.10-1. Level detector.

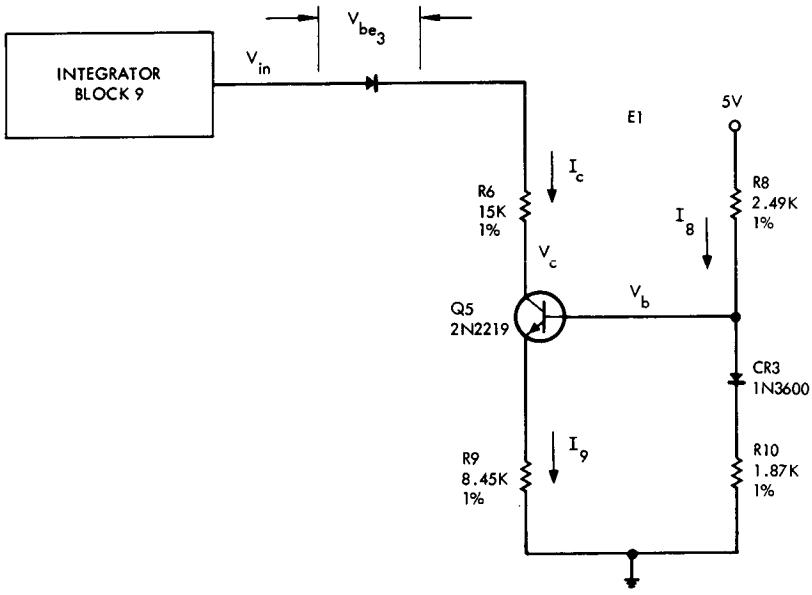


Figure 5.10-2. Current source model.

where,

$$I_{8\ min} = \frac{E_1 - V_{CR_3\ max}}{R_{8\ min} + R_{10\ max}} = 1.02\ ma. \quad (5.10\text{-}5)$$

Substituting into Eq. (5.10-3) yields

$$I_{c\ max} = 275\ \mu amp.$$

The minimum integrator voltage, $V_{in\ min}$, is determined by the D.C. level, the current sensing amplifier output frequency and the ramp rate as shown in Figure 5.10-3.

$$V_{in\ min} = V_{dc_{min}} + \frac{\bar{K}_{max}}{2} \frac{1}{f_{min}} \quad (5.10\text{-}6)$$

where

$$\bar{K}_{max} = -363\ volts/sec \quad (5.9\text{-}10)$$

$$f_{min} = 200\ Hz$$

Substituting into Eq. (5.10-6) yields

$$V_{in\ min} = 8\ volts - 0.84\ volts = 7.16\ volts.$$

Note that $V_{in\ min}$ has been normalized to fit the model of Figure 5.10-2.

Substituting into Eq. (5.10-2) yields

$$V_{c\ min} = 2.21\ volts. \quad (5.10\text{-}7)$$

From Eq. (5.10-1),

$$V_{c\ min} = 2.21 > 2.2\ volts = V_{b\ max} - V_{be_{5\ min.}} \quad (5.10\text{-}8)$$

The above indicates that Q_5 will not saturate; however, it is marginal. Therefore, the suggestion is made that R_8 be increased to approximately an 8K, 1 percent, 1/8 watt resistor, thus lowering $V_{b\ max}$. R_9 will have to be adjusted to allow 200 μamps to flow in the collector circuit.

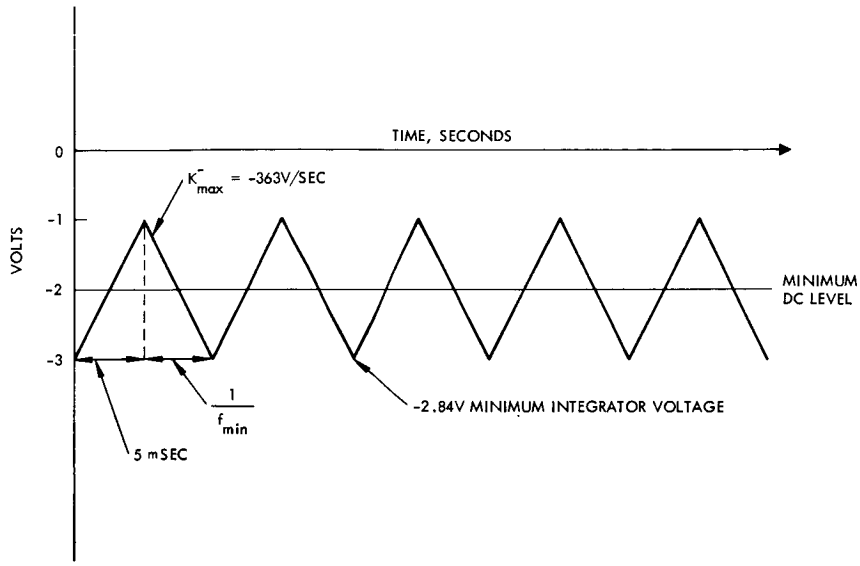


Figure 5.10-3. Worst-case integrator output.

Transistors Q_1 and Q_2 should be "off" until the minimum normal integrator voltage has been exceeded. Since both sides of the amplifier are the same, analysis will be carried out for only one transistor, Q_2 (Figure 5.10-4).

From Figure 5.10-4, Q_2 will be "off" as long as:

$$V_{b_{2\,min}} > E_{3\,max} - V_{be_{2\,min}} = 4.5 \text{ volts} \qquad (5.10\text{-}9)$$

$$V_{b_{2\,min}} = V_{in\,min} A_{max} + E_{2\,min} - V_{CR_{2\,max}} - I_{4\,max} R_{4\,max} \qquad (5.10\text{-}10)$$

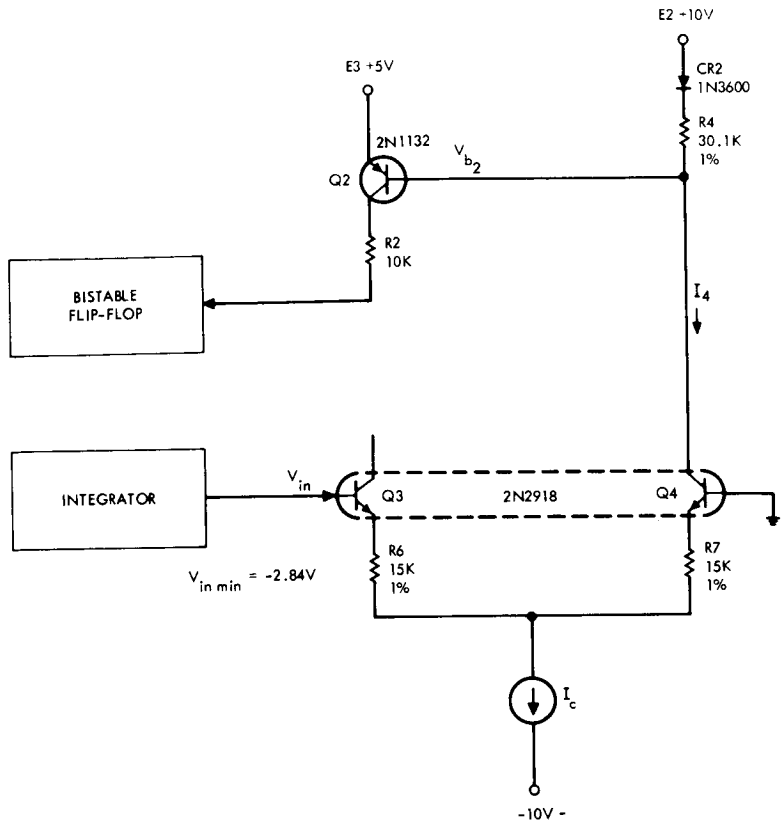


Figure 5.10-4. Reduced level detector model.

where,

A = voltage gain of the differential amplifier.

$$A_{max} = \frac{-R_{4\ max}}{(R_6 + R_7)\ min} = -1.12 \qquad (5.10\text{-}12)$$

$$I_{4\ max} = \frac{I_{c\ max}}{2} = 138\ \mu amp \qquad (5.10\text{-}13)$$

Substituting into Eq. (5.10-10) yields

$$V_{b_{2\ min}} = 1.77\ volts. \qquad (5.10\text{-}14)$$

From Eq. (5.10-9),

$$V_{b_{2\ min}} = 1.77\ volts \not> 4.5\ volts = E_{3\ max} - V_{be_{2\ min}} \qquad (5.10\text{-}15)$$

Therefore, Q_2 will turn "on" before $V_{in\ min}$ is reached. This can be corrected by reducing the gain of the amplifier. If R_3 and R_4 are changed to 16.9K, 1 percent, 1/8 watt resistors, then

$$A_{max} = 0.62$$

$$V_{b_{2\ min}} = 5.09 \text{ volts}$$

From Eq. (5.10-9),

$$V_{b_{2\ min}} = 5.09 \text{ volts} > 4.5 \text{ volts}$$

$$= E_{3\ max} - V_{be_{2\ min}} \qquad (5.10\text{-}16)$$

The integrator voltage, which will turn "on" Q_2, is found by solving Eq. (5.10-10) for $V_{in\ min}$ and letting $V_{b_{2\ min}} = 4.5$ volts.

$$V_{in\ min} = \frac{V_{b_{2\ min}} - E_{2\ min} + V_{CR_{2\ max}} + I_{4\ max} R_{4\ max}}{A_{max}} \qquad (5.10\text{-}17)$$

Q_2 turn "on" voltage is

$$V_{in\ min} = -3.8 \text{ volts}$$

It follows that Q_1 turn "on" voltage is +3.8 volts.

5.10.1 Conclusions

The level detector will work under worst-case conditions if the above changes are incorporated into the design.

5.10.2 Stress Analysis

A worst-case analysis was performed to insure that no component was over-stressed. A table of these results can be found in Table 5.10-2.

Symbol	Minimum	Maximum
E_1	4.8 volts	5.2 volts
E_2	9.9 volts	10.1 volts
E_3	4.9 volts	5.1 volts
R_4	28.6K	31.6K
R_6	14.2K	15.8K
R_7	14.2K	15.8K
R_8	2.36K	2.99K
R_9	8.01K	
R_{10}		1.96K
V_{CR_2}		0.6 volt
V_{CR_3}		0.6 volt
V_{be_2}	0.6 volt	
V_{be_3}		0.6 volt
V_{be_5}	0.6 volt	
V_{DC}	-2 volts	

Table 5.10-1. Table of critical parameters for block 10.

5.11 BLOCK 11, SWITCHING REGULATOR AND BIAS CONVERTER

The switching regulator and bias converter (Figure 5.11-1) provides the bias voltages for all the other circuitry. This block is a standard design and has been proven in the past. For this reason, a worst-case study was not attempted. A stress analysis was performed, however, to insure that all components were operating within permissible stress levels A summary of the results is found in Table 5.11-1.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation (mw)*			Power Dissipation (mw)*		
Transistors			Vceo (volts)			Vceo (volts)	
Q_1 and Q_2	2N1132	1 watt	35		<1	10	
Q_3 and Q_4	2N2918	250	45		1	10	
Q_5	2N2219	800	40		1	5	
Resistors							
R_1	10K	250			<1		
R_2	10K	250			<1		
R_3	16.9K	125			<1		
R_4	16.9K	125			<1		
R_5	10K	250			2		
R_6	15K	125			<1		
R_7	15K	125			<1		
R_8	2.49K	125			3		
R_9	8.45K	125			<1		
R_{10}	1.87K	125			2		
			PIV	I_f		PIV	I_f
Diodes			(volts)	(ma)		(volts)	(ma)
CR_1 and CR_2	1N3600	500	50	200	<1	0	0.2
CR_3	1N3600	500	50	200	1	0	1.15

*Unless otherwise noted.

Table 5.10-2. Stress analysis summary for block 10.

Component Designation	Type	Rating		Actual Stress	
		Power Dissipation (mw)*		Power Dissipation (mw)*	
Transistors			Vceo (volts)		Vceo (volts)
Q_1 and Q_2	2N2893	17 watts	80	35	20
Q_{3A} and Q_{3B}	2N2918	250	45	2	5
Q_4	2N1132	1 watt	35	<1	15
Q_5	2N1132	1 watt	35	9	20
Q_6	2N2219	800	40	9	15
Q_{7A} and Q_{7B}	2N3810	600	90	<1	5
Q_8	2N2219	800	40	2	20
Q_9	2N2219	800	40	1	5
Q_{10}	2N2893	17 watts	80	193	40
† Q_{11}	2N1132	1 watt	35	<1	40
** Q_{11}	2N2905A	600	60	<1	40
Resistors					
R_1	100	250			
R_2	100	250			
R_3	240	250		40	
R_4	100	250		<1	

*Unless otherwise noted.
**Recommended change.
†Overstressed

Table 5.11-1. Stress analysis summary for block 11.

Component Designation	Type	Rating		Actual Stress	
		Power Dissipation (mw)*		Power Dissipation (mw)*	
R_5	240	250		40	
R_6	976	125		<1	
R_7	40.2K	125		<1	
R_8	22.6K	125		1	
R_9	40.2K	125		<1	
R_{10}	100K	250		<1	
R_{11}	3.83K	125		2	
R_{12}	3.74K	125		2	
R_{13}	3.16K	125		<1	
R_{14}	1.21K	125		1	
R_{15}	1.82K	250		11	
R_{16}	8.60K	125		3	
R_{17}	6.40K	125		2	
R_{18}	100	250		<1	
R_{19}	6.40K	125		2	
R_{20}	1K	250		<1	
R_{21}	2.49K	125		10	
R_{22}	301	125		<1	
R_{23}	19.6K	125		20	
R_{24}	1.5K	250		20	

*Unless otherwise noted.

Table 5.11-1 (continued). Stress analysis summary for block 11.

Component Designation	Type	Rating			Actual Stress		
		Power Dissipation (mw)*			Power Dissipation (mw)*		
R_{25}	10K	250			2		
R_{26}	240	250			33		
R_{27}	510	250			17		
R_{28}	1K	250			5		
R_{29}	10K	250			<1		
R_{30}	1K	250			<1		
			PIV	I_f		PIV	I_f
Diodes			(volts)	(ma)		(volts)	(ma)
$CR_{1,2,3,4}$	1N3600	500	50	200	2.5	10	
$CR_{5,6,7,8}$	1N3879	3 watts	50	6 amp	120	5	
$CR_{9,10,11}$							
CR_{12}	1N3600	500	50	200	6	5	
CR_{13}	1N3730				11	20	18
$CR_{14,15}$	1N3600	500	50	200	<1	0	0.1
CR_{16}	1N825				47	6.2	7
CR_{17}	1N3600	500	50	200	<1	0	0.6
CR_{18}	1N3600	500	50	200	1	3	26
CR_{19}	1N3889				105	40	350

*Unless otherwise noted.

Table 5.11-1 (continued). Stress analysis summary for block 11.

Component Designation	Type	Rating		Actual Stress	
	μf	Power Dissipation (mw)*		Power Dissipation (mw)*	
Capacitors			(volts)		(volts)
C_1	10		20		10
C_2	10		20		10
C_3	100		20		5
C_4	100		20		5
C_5	10		20		10
C_6	10		20		10
C_7	10		20		5
C_8	10		20		5
C_9	100		20		5
C_{10}	100		20		5
C_{11}	10		20		20
C_{12}	47		50		20
C_{13}	33		75		20
C_{14}	10		20		5
C_{15}	10		20		5
C_{16}	100		20		5
C_{17}	1		35		4
C_{18}	10		20		5
C_{19}	33		75		40
C_{20}	10		50		40

*Unless otherwise noted.

Table 5.11-1 (continued). Stress analysis summary for block 11.

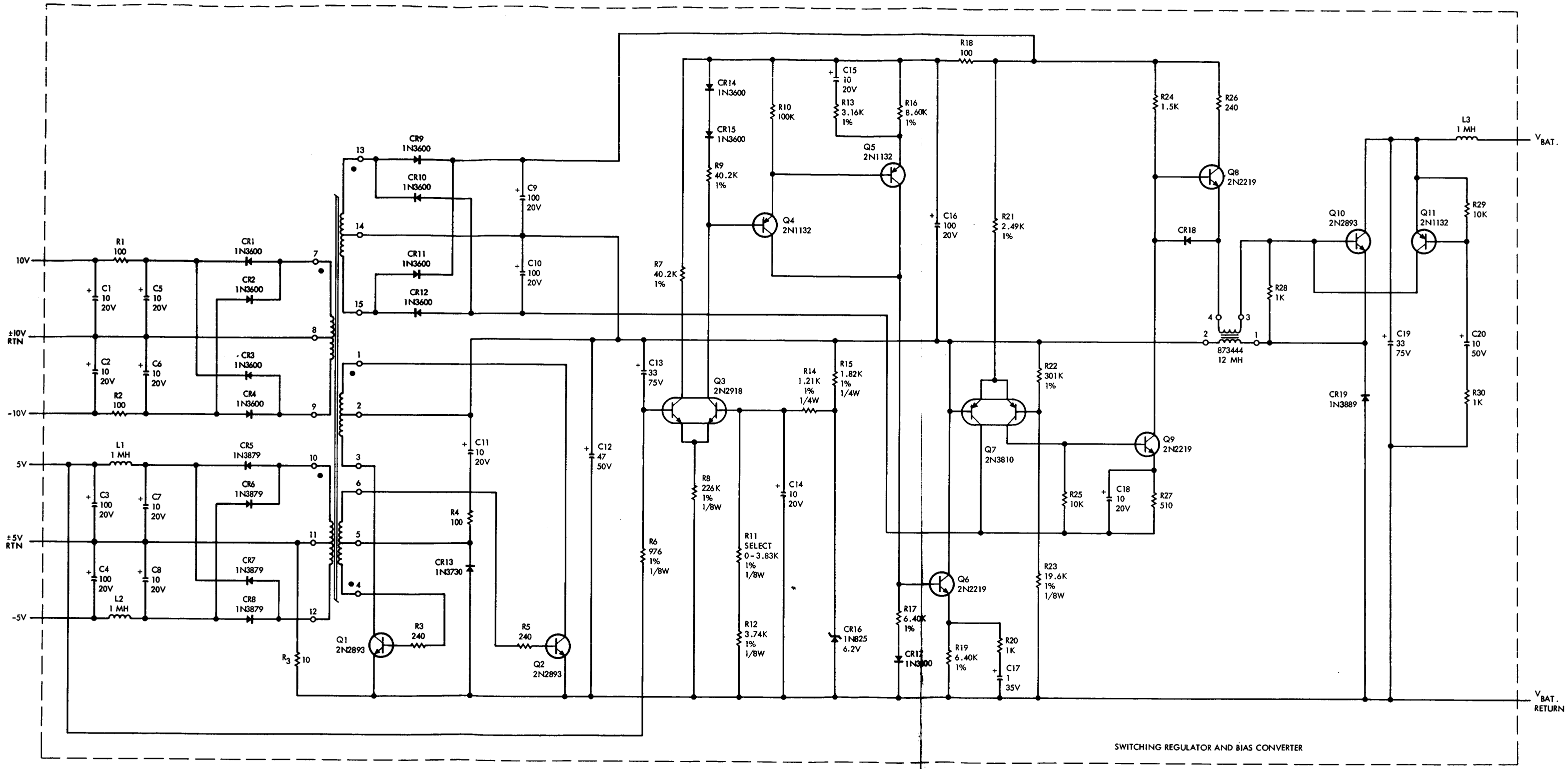


Figure 5.11-1. Switching regulator and bias converter.

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